User Manual

APM32E030x8

Arm® Cortex® -M0+ based 32-bit MCU

Version: V1.0

Contents

1 Introduction and Document Description Rules

1.1 Introduction

This reference manual provides application developers with all the information about how to use MCU (micro-controller) system architecture, memory and peripherals.

For information about Arm® Cortex® -M0+ core, please refer to *Arm® Cortex® -M0+ Technical Reference Manual*; please refer to the corresponding datasheet for detailed data such as model information, dimension and electrical characteristics of the device; for all MCU series models, please refer to the corresponding data manual for memory mapping, peripheral existence and their number.

It is hereby declared that Geehy Semiconductor Co., Ltd., hereinafter refer to as "Geehy".

1.2 Document Description Rules

1.2.1 "Register Functional Description" Rules

（1） Control (CTRL) registers are all "set to 1 and cleared by software", unless otherwise specified.

（2） The control registers are usually followed by verb abbreviations to make a distinction. The verbs can be: EN-Enable, CFG-Configure, D-Disable, SET-Setup and SEL-Select

（3） The state register abbreviation is usually followed by FLG to make a difference.

（4） The value and data registers usually include V, VALUE, D and DATA, which are not followed by verbs, such as: xxPSC and CNT.

1.2.2 Full Name and Abbreviation Description of Terms

Table 1 R/W Abbreviation and Description

R/W	Description	Abbreviation
read/write	Software can read and write this bit.	R/W
read-only	Software can only read this bit.	R
write-only	Software can only write this bit, and after reading this bit, the reset value will be returned.	W
read/clear	The software can read this bit and clear it by writing 1. Writing 0 has no effect on this bit.	RC_W1
read/clear	The software can read this bit and clear it by writing 0. Writing 1 has no effect on this bit.	RC_W0
read/clear by read	The software can read this bit, reading this bit will automatically clear it to 0, and writing this bit is invalid.	RC_R
read/set	The software can read and set this bit, and writing 0 has no effect on this bit.	R/S
read-only write trigger	The software can read this bit and writing 0 or 1 can trigger an event but has no effect on the value of this bit.	RT_W
toggle	The software can flip this bit only by writing 1 and writing 0 has no effect on this bit.	T

Table 2 Functional Description and Full Name and Abbreviation of Terms of Commonly Used Registers

Full name in English	English abbreviation
Enable	EN
Disable	D
Clear	CLR
Select	SEL
Configure	CFG
Contrl	CTRL
Controller	C
Reset	RST
Stop	STOP
Set	SET
Load	LD
Calibration	CAL
Initialize	INIT
Error	ERR
Status	STS
Ready	RDY
Software	SW
Hardware	HW
Source	SRC
System	SYS
Peripheral	PER
Address	ADDR
Direction	DIR
Clock	CLK
Input	I
Output	O
Interrupt	INT
Data	DATA
Size	SIZE
Divider	DIV
Prescaler	PSC

Full name in English	English abbreviation
Multiplier	MUL
Period	PRD

Table 3 Full Name and Abbreviation of Modules

Full name in English	English abbreviation
Reset and Clock Management	RCM
Power Management Unit	PMU
Nested Vector Interrupt Controller	NVIC
External Interrupt /Event Controller	EINT
Direct Memory Access	DMA
Debug MCU	DBG MCU
General-Purpose Input Output Pin	GPIO
Alternate Function Input Output Pin	AFIO
Timer	TMR
Watchdog Timer	WDT
Independent Watchdog Timer	IWDT
Windows Watchdog Timer	WWDT
Real-Time Clock	RTC
Universal Synchronous Asynchronous Receiver Transmitter	USART
Inter-integrated Circuit Interface	I2C
Serial Peripheral Interface	SPI
Inter-IC Sound Interface	I2S
Analog-to-Digital Converter	ADC
Cyclic Redundancy Check Calculation Unit	CRC

2 System Architecture

2.1 Full Name and Abbreviation Description of Terms

Table 4 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Advanced High-Performance Bus	AHB
Advanced Peripheral Bus	APB

2.2 System Architecture Block Diagram

The main system mainly consists of two master modules and four slave modules. The main modules are Arm® Cortex® -M0+ core and general-purpose DMA. The slave modules are internal SRAM, internal flash memory Flash, AHB2 bus connecting all GPIO ports, and AHB1/APB bridges on AHB1 bus, among which, AHB1/APB bridges connect all peripherals.

These are connected through a multi-level AHB bus architecture, as shown in the figure below:

Figure 1 APM32E030x8 System Architecture Block Diagram

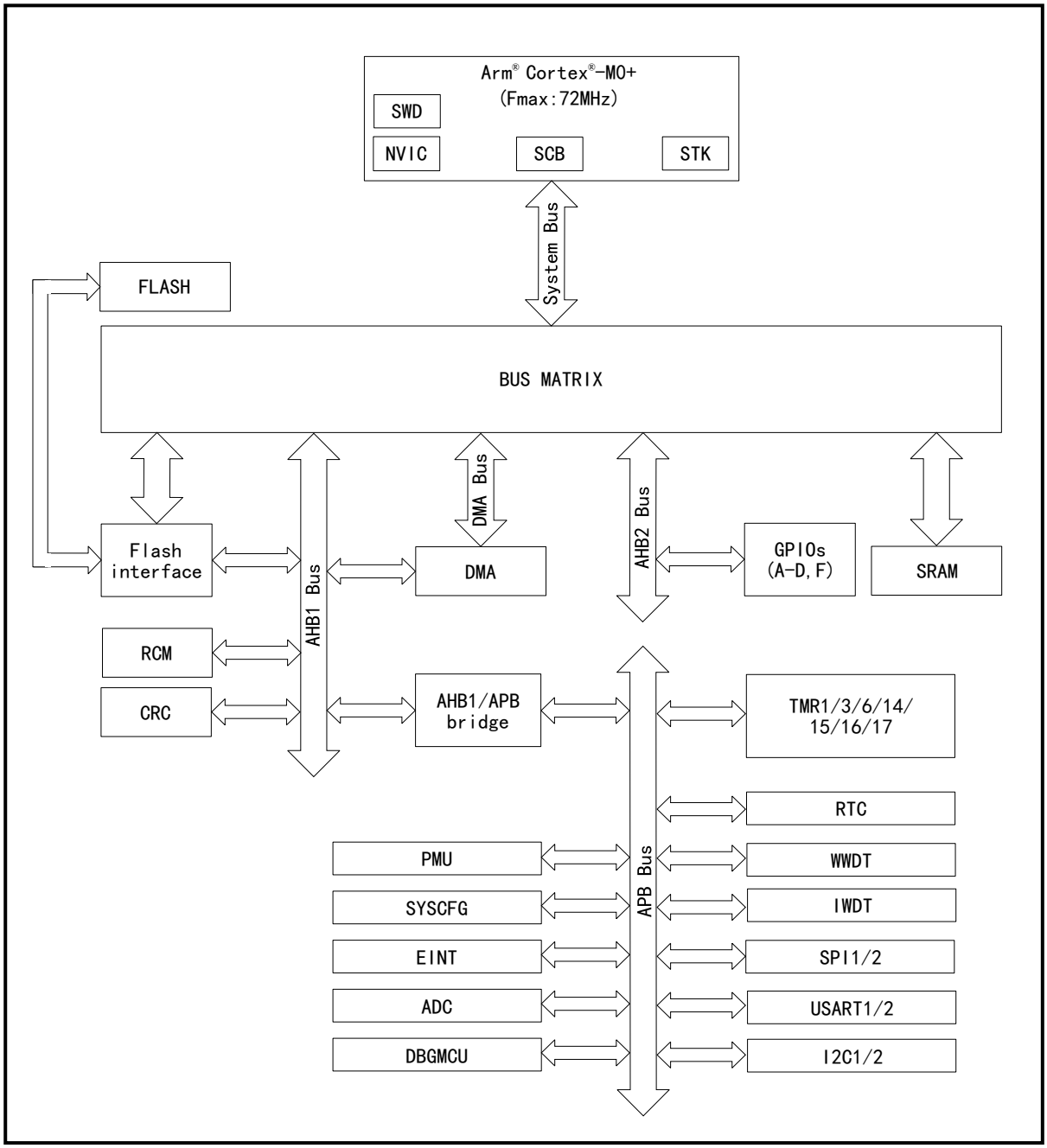


Table 5 Bus Name

Name	Instruction
System bus	Connect the system bus (peripheral bus) of Arm® Cortex® -M0 core and the bus matrix.
DMA bus	Connect AHB master control interface of DMA and the bus matrix.
Bus matrix	Coordinate the access of the core and DMA; consist of CPU AHB, system bus, DMA bus and FMC, SRAM, AHB2 and AHB1/APB bridge. AHB peripheral is connected with the system bus through the bus matrix and is allowed to access DMA.

Name	Instruction
AHB/APB bridge	The bridge provides synchronous connection between AHB and APB buses. The non-32-bit access to APB register will be converted into 32 bits automatically.

2.3 Memory Mapping

The memory mapping address is totally 4GB address. The assigned addresses include the core (including core peripherals), on-chip Flash (including main memory area, system memory area and option bytes), on-chip SRAM, and bus peripherals (including AHB and APB peripherals). Please refer to the data manual of the corresponding model for specific information of various addresses.

2.3.1 Embedded SRAM

Built-in static SRAM. It can access by byte, half word (16 bits) or full word (32 bits). The start address of SRAM is 0x2000 0000.

2.4 Startup Configuration

APM32F MCU series realizes a special mechanism. By configuring the BOOT pin parameter and the nBOOT1 bit in FMC_OBCS, there are three different startup modes, namely, the system can not only start from Flash memory or system memory, but also start from the built-in SRAM. The memory selected as the start zone is determined by the selected startup mode.

2.4.1 Configuring the Boot Mode

Table 6 Startup Mode Configuration and Access Mode

Startup mode selection pin		Startup mode	Access mode
BOOT1	BOOT0		
X	0	Main flash memory（Flash）	The main flash memory is mapped to the boot space, but it can still be accessed at its original address, that is, the contents of the flash memory can be accessed in two address areas.
0	1	System memory	The system memory is mapped to the boot space (0x0000 0000), but it can still be accessed at its original address.
1	1	Built-in SRAM	SRAM can be accessed only at the starting address.

Note:

（1） The boot space address is 0x0000 0000

（2） The original address of Flash is 0x0800 0000

（3） The original address of system memory is 0x1FFF EC00

（4） The starting address of SRAM is 0x2000 0000

（5） The value of BOOT1 is negation of nBOOT1 option bit

The user can select the startup mode after reset by setting the states of BOOT1 (configuration nBOOT1) and BOOT0 pins.

BOOT pin should keep the user's required startup configuration in standby mode. When exiting from the standby mode, the value of boot pin will be latched.

If you choose to start from built-in SRAM, you must use NVIC's exception table and offset register to remap the vector table to SRAM when writing the application code.

2.4.2 Embedded startup program

The embedded startup program is written on the production line by Geehy and stored in the system memory area.

3 FLASH Memory

This chapter mainly introduces the storage structure, read, erase, write, read/write protection, unlock/lock characteristics of Flash, and the involved register functional description.

3.1 Full Name and Abbreviation Description of Terms

Table 7 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Flash Memory Controller	FMC

3.2 Main Characteristics

（1） Flash memory structure

- Contain main memory area and information block
- The capacity of main memory area is up to 64KB
- The information block is divided into system memory area and option byte
- The system storage capacity is 3KB, storing the BootLoader program, 96-bit unique UID, and primary storage capacity information
- The capacity of the option byte area is 16Bytes

（2） Functional Description

- Read Flash
- Page/Mass erase Flash
- Write Flash
- Read/Write protection Flash
- Configure option bytes

3.3 Flash Memory Structure

Table 8 Flash Memory Structure of APM32F030x4x6x8 Series Products

Block	Name	Address area	Size (byte)	Sector
Main memory area	Page 0	0x0800 0000–0x0800 03FF	1K	Sector 0
Main memory area	Page 1	0x0800 0400–0x0800 07FF	1K	
Main memory area	Page 2	0x0800 0800–0x0800 0BFF	1K	
Main memory area	Page 3	0x0800 0C00–0x0800 0FFF	1K	
Main memory area	…	…	…	…
Main memory area	Page 62	0x0800 F800–0x0800 FBFF	1K	Sector 15

Block	Name	Address area	Size (byte)	Sector
Main memory area	Page 63	0x0800 FC00–0x0800 FFFF	1K	
Information block	System memory area	0x1FFF EC00–0x1FFF F7FF	3K	-
Information block	Option byte	0x1FFF F800–0x1FFF F80F	16	-

Note: The number of pages in the main memory block of APM32E030x8 series products is related to the Flash capacity of specific product.

3.4 Functional Description

Describe the operation of main memory and information block (including system memory area and option byte), including read, write, erase and read/write protection.

Reading Flash includes main memory block and information block, while the erase, write, read/write are introduced separately; the system memory area has been written before the product leaves the factory and cannot be modified by the user. The erase, write, and read/write protection of the module will not be introduced.

3.4.1 Read Flash

Flash memory can be directly addressed, and reading Flash is affected by the following configuration:

Wait cycle

Different wait cycles should be configured for different system clocks:

- 0 wait cycle: 0<system clock≤24MHz
- 1 wait cycle: 24MHz<system clock≤48MHz
- 2 wait cycle: 48MHz<system clock≤72MHz

Prefetch buffer

It can improve the reading speed and every time it is reset, the prefetch buffer will be automatically opened; the read interface with prefetch buffer. It can be configured only when the system clock is consistent with AHB clock and is less than 24MHz, and can be used only when the system clock is consistent with AHB clock.

3.4.2 Main Memory Block

3.4.2.1 Erase main memory block

FMC supports page erase and mass erase (full erase) to initialize the contents of the main memory area to high level (the data is represented as 0xFFFF). Before writing to Flash, users are advised to erase the write address page. If the data of write address is not 0xFFFF, a programming error will be triggered.

Main memory page erase

Page erase is an independent erase according to the main memory area page selected by the program, which will not have any impact on the page not selected for erasure.

After the correct page erase (or flash write operation) is completed, OCF of FMC_STS register will be set. If OCIE interrupt is enabled, an operation completion interrupt will be triggered. Users need to note that the page to be erased must be a valid page (the valid address of the main memory area and the address not protected by write).

Main memory mass erase

The mass erase operation will erase all the contents in the main storage area of Flash, so the users need to pay special attention when using it to avoid the loss of important data caused by misoperation.

3.4.2.2 Write main memory block

FMC supports the writing of 16-bit (half word) data in the main memory area. You can select Debug, BootLoader, program running in SRAM, and directly reading the erased page to judge whether the erasing is successful.

In order to ensure correct writing, it is necessary to check whether the destination address has been erased before writing; if it is not erased, the written data will be invalid and PEF bit of FMC_STS register will be set to "1". If the destination address has write protection, the written data is invalid and a write protection error will be triggered (WPEF bit of FMC_STS is set to "1").

3.4.2.3 Main memory block of read/write protection

Read/Write protection of the flash is used to prevent illegal reading/modification of the main memory area code or data, and it is controlled by the read/write protection configuration byte of option byte. For APM32E030x8 series products, the basic unit of write protection is 4 pages (i.e. KB).

Read protection

The read protection has three levels, namely, Level 0, Level 1 and Level 2, which are specifically described as follows:

Table 9 Difference among Read Protection Levels

Category	READPROT	Description
Level 0	0xAA	The main memory area and option byte are erasable, writable and readable.
Level 1	Other values except 0xAA and 0xCC	User mode: Allowed to erase, write and read the main memory area and option byte. Debug, SRAM running, system memory area running: Access to the main memory area is disabled; the option byte is erasable, writable and readable, but when the level is modified to 0, the main memory area erase will be performed first.
Level 2	0xCC	Cannot Debug, SRAM run, system storage run, allow to erase, write, read primary storage, allow to read option bytes, allow to write option bytes outside the read protection level, do not allow to erase option bytes.

Write protection

Write protection control can be conducted for the corresponding page of the main memory block by configuring the value of write protection option byte WRP0/1/2/3. After the write protection is turned on, the content on the corresponding page of the main memory area cannot be modified in any way.

3.4.2.4 Main memory block of unlock/lock

FMC_CTRL1 of the reset FMC will be locked by hardware, and then FMC_CTRL1 can't be directly written, and the corresponding value must be written to FMC_KEY according to the correct sequence to unlock FMC. The KEY value is

as follows:

- KEY1=0x45670123
- KEY2=0xCDEF89AB

The wrong writing sequence or wrong value will cause the program to enter the hardware wrongly. At this time, FMC will be locked, and all FMC operations will be invalid until it is reset next time. The users can also lock FMC through software by writing "1" to LOCK bit of the control register 2 (FMC_CTRL2).

In each Flash programming operation, the users must follow the steps of "Flash unlock - program by user - Flash lock", so as to avoid the risk that user code/data is accidentally modified due to the Flash unlocking after the Flash programming operation.

3.4.3 Option Byte

3.4.3.1 Erase option byte

Support erase function. After the correct option byte erase (or option byte write operation) is completed, OCF of FMC_STS register will be set. If OCIE interrupt enable is enabled, an operation completion interrupt will be triggered.

3.4.3.2 Write option byte

Eight configurable bytes of option bytes all support writing function.

3.4.3.3 Option byte of write protection

By default, the option byte is always readable and write protected. To perform write operation (program/erase) for the option byte block, first write the correct key sequence (the same as that of locking) in FMC_OBKEY, and then allow the write operation of option byte block; the OBWEN bit of FLASH_CTRL2 register indicates write enabled; clear this bit and write operation will be disabled.

3.4.3.4 Unlock/Lock option byte

After the system reset, the option byte is locked by default. Only when the option byte is unlocked correctly, can it be modified. The difference between option byte unlocking and flash unlocking is that FMC_OBKEY register rather than FMC_KEY register writes the KEY value. The option byte does not support "software lock". The user should pay special attention to that the value of the modified option byte is not loaded after the system reset. If the option byte is loaded again, it must be powered on or reset the OBLOAD position "1" of the register FMC_CTRL2 to make it take effect.

3.4.4 Functional Description of Option Byte

The option byte provides some optional functions for users, and it mainly consists of 8 configurable bytes and corresponding complementary codes. Every time the up power reset, the option byte area will be reloaded to the FMC_ OBCS and FMC_WRTPROT register (the option byte will only take effect each time they are reloaded to FMC). In the process of reloading, if a certain configurable byte does not match its reverse code, an option byte error (OBE bit of FMC_ register is set to "1") will be triggered, and this byte will be set to "0xFF". The information of 16 bytes in the option byte area is shown in the table below.

Table 10 Option Bytes

Address	Option byte	Initial value	R/ W	Functional description
0x1FFF F800	READPROT	0xA5	R/ W	Read protection configuration Bit [7:0]: READPROT

Address	Option byte	Initial value	R/W	Functional description
				0xAA: Level 0 0xCC: Level 2 Others: Level 1
0x1FFF F801	nREADPROT	0x5A	R	READPROT complementary code
0x1FFF F802	UOB	0xFF	R/W	User option byte Bit 0: WDTSEL 0: Hardware watchdog 1: Software watchdog Bit 1: nRSTSTOP 0: Reset occurs when entering the Stop mode 1: Reset does not occur when entering the Stop mode Bit 2: nRSTSTB 0: Reset occurs when entering the Standby mode 1: Reset does not occur when entering the Standby mode Bit 3: Reserved Bit 4: nBOOT1 Select BOOT mode Bit 5: VDDAMONI 0: V_{DDA} power supply detector is disabled 1: V_{DDA} power supply detector is enabled Bit 6: SRAMPARITY 0: RAM parity check is disabled 1: RAM parity check is enabled Bit 7: Reserved
0x1FFF F803	nUOB	0x00	R	UOB complementary code
0x1FFF F804	Data0	0xFF	R/W	User data byte 0
0x1FFF F805	nData0	0x00	R	Data0 complementary code
0x1FFF F806	Data1	0xFF	R/W	User data byte 1
0x1FFF F807	nData1	0x00	R	Data complementary code
0x1FFF F808	WRP0	0xFF	R/W	Write protection configuration 0
0x1FFF F809	nWRP0	0x00	R	WRP0 complementary code
0x1FFF F80A	WRP1	0xFF	R/W	Write protection configuration 1
0x1FFF F80B	nWRP1	0x00	R	WRP1 complementary code
0x1FFF F80C	WRP2	0xFF	R/W	Write protection configuration 2
0x1FFF F80D	nWRP2	0x00	R	WRP2 complementary code
0x1FFF F80E	WRP3	0xFF	R/W	Write protection configuration 3
0x1FFF F80F	nWRP3	0x00	R	WRP3 complementary code

Note: When the configurable byte and its reverse code value are "0xFF", the match will not be verified in the reloading process

Table 11 Write Protection WRPx Function Description of Main Memory Area

Product capacity	Functional description
APM32E030x8 series products	Each bit in WRPx controls the write protection of 4KB (4 pages) address of the main memory area 0: Write protection is turned on 1: Write protection is not turned on WRP0: Page 0-31 WRP1: Page 32-63

Note: Flash read/write protection configuration is independent of each other. Removing the write protection will not force the loss of the contents of the main memory area, but keep them as they are.

3.5 FMCRegister Address Mapping

Base address: 0x40022000

Table 12 FMC Register Address Mapping

Register name	Description	Offset address
FMC_CTRL1	Control register 1	0x00
FMC_KEY	Key register	0x04
FMC_OBKEY	Option byte key register	0x08
FMC_STS	State register	0x0C
FMC_CTRL2	Control register 2	0x10
FMC_ADDR	Address register	0x14
FMC_OBCS	Option byte control/state register	0x1C
FMC_WRTPROT	Write protection register	0x20

3.6 Register Functional Description

3.6.1 Control register 1 (FMC_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	WS	R/W	Wait State Configure 000: 0 wait cycle, 0<system clock≤24MHz 001: 1 wait cycle: 24MHz<system clock≤48MHz 010: 2 wait cycle: 48MHz<system clock≤72MHz Others: Reserved
3	Reserved		
4	PBEN	R/W	Prefetch Buffer Enable 0: Disable 1: Enable
5	PBSF	R	Prefetch Buffer Status Flag 0: In disabled state 1: In enabled state

Field	Name	R/W	Description
31:6	Reserved		

3.6.2 Key register (FMC_KEY)

Offset address: 0x04

Reset value: xxxx xxxx

Field	Name	R/W	Description
31:0	KEY	W	FMC Key Writing the keys represented by these bits can unlock FMC. These bits can only perform write operation, and 0 is returned when read operation is performed.

3.6.3 Option byte key register (FMC_OBKEY)

Offset address: 0x08

Reset value: xxxx xxxx

Field	Name	R/W	Description
31:0	OBKEY	W	Option Byte Key Writing the keys represented by these bits can unlock the option byte write operation. These bits can only perform write operation and 0 is returned when read operation is performed.

3.6.4 State register (FMC_STS)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	BUSYF	R	Busy Flag This bit indicates that a flash operation is in progress. These bits can only perform write operation, and 0 is returned when read operation is performed.
1	Reserved		
2	PEF	RC_W1	Programming Error Flag This bit will be set by software when the value before the address is edited is not "0xFFFF". Write 1 to clear zero. Before starting the programming operation, you should reset the STA bit in the FMC_CTRL2 register.
3	Reserved		
4	WPEF	RC_W1	Write Protection Error Flag This bit will be set by hardware when programming the write protection address in FLASH.
5	OCF	RC_W1	Operation Complete Flag This bit will be set by hardware when read/write operation in FLASH is completed.
31:6	Reserved		

3.6.5 Control register 2 (FMC_CTRL2)

Offset address: 0x10

Reset value: 0x0000 0080

Field	Name	R/W	Description
0	PG	R/W	Program Set this bit to 1 to program Flash
1	PAGEERA	R/W	Page Erase Set this bit to 1 to erase the page
2	MASSERA	R/W	Mass Erase Set this bit to 1 to erase the mass.
3	Reserved		
4	OBP	R/W	Option Byte Program Set this bit to 1 to program the option byte.
5	OBE	R/W	Option Byte Erase Set this bit to 1 to erase the option byte.
6	STA	R/W	Start Erase This bit can be only set to 1 by software, and can be reset by clearing STS_BUSYF bit.
7	LOCK	R/W	Lock This bit can be written to 1 only, and when this bit is set to 1, it means that FMC and CTRL2 registers are locked. This bit is reset by the hardware after the unlocking sequence is detected.
8	Reserved		
9	OBWEN	R/W	Option Byte Write Enable When this bit is set to 1, the option byte can be programmed.
10	ERRIE	R/W	Error interrupt Enable 0: Interrupt is disabled 1: Interrupt is enabled When STS_PEF=1 or STS_WPEF=1, set this bit to generate an interrupt.
11	Reserved		
12	OCIE	R/W	Operation Complete Interrupt Enable 0: Operation completion interrupt is disabled 1: Operation completion interrupt is enabled If this bit is set, when STS_OCF=1, an interruption can be generated.
13	OBLOAD	R/W	Force Option Byte Load When this bit is set to 1, force to reload the option byte to generate system reset. 0: Idle 1: Force to load
31:14	Reserved		

3.6.6 Address register (FMC_ADDR)

Offset address: 0x14

Reset value: 0x0000 0000

The register is changed to currently/finally used address by hardware; in page erasing, the register needs to be configured by software.

Field	Name	R/W	Description
31:0	ADDR	W	Flash Address In programming operation, the bit is written to the address to be programmed; in page erasing, this bit is written to the page to be erased.

3.6.7 Option bye control/state register (FMC_OBCS)

Offset address: 0x1C

Reset value: 0xXXXX XX0X

The reset value of the register is related to the value in the written option byte; the reset value of OBE bit is related to the result whether the value of the loaded option byte is consistent with its reverse code.

Field	Name	R/W	Description
0	OBE	R	Option Byte Error 1: The loaded option byte does not match its complementary code. The option byte and its complementary code are forced to write to 0xFF
2:1	READPROT	R	Indicate which level of read protection was enabled. If bit1 is set to 1, it is level 1. If bit2 is set to 1, it is level 2. 00: Level 0 01: Level 1 1X: Level 2
7:3	Reserved		
8	WDTSEL	R	Watchdog Select 0: Hardware watchdog 1: Software watchdog
9	RSTSTOP	R	nReset in STOP Mode 0: Generate 1: Not generate
10	RSTSTDB	R	nReset in STANDBY Mode 0: Generate 1: Not generate
11	Reserved		
12	nBOOT1	R	nBoot1 Mode Configure
13	VDDAMONI	R	V_{DDA} Monitor
14	SRAMPARITY	R	SRAM Parity Check
15	Reserved		
23:16	DATA0	R	Data0
31:24	DATA1	R	Data1

3.6.8 Write protection register (FMC_WRTPROT)

Offset address: 0x20

Reset value: 0xXXXX XXXX (the reset value depends on the programming value in option bye)

Field	Name	R/W	Description
31:0	WRTPROT	R	Write Protect 0: Valid 1: Invalid

4 System Configuration Controller (SYSCFG)

4.1 Full Name and Abbreviation Description of Terms

Table 13 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Fast Mode Plus	FM+
System Configuration Controller	SYSCFG

SYSCFG is mainly used to manage address mapping and control interrupts, specifically: controlling the fast mode plus of I2C on some IO ports; DMA trigger source remapping of TMR16, TMR17, USART1 and ADC; remapping from memory to code start area; and managing the external interrupts connected to GPIO.

For details of related configuration, see SYSCFG register configuration.

4.2 Register Address Mapping

Table 14 SYSCFG Register Address Mapping

Register name	Description	Offset address
SYSCFG_CFG1	Configuration register 1	0x00
SYSCFG_EINTCFG1	External interrupt register 1	0x08
SYSCFG_EINTCFG2	External interrupt register 2	0x0C
SYSCFG_EINTCFG3	External interrupt register 3	0x10
SYSCFG_EINTCFG4	External interrupt register 4	0x14
SYSCFG_CFG2	Configuration register 2	0x18

4.3 Register Functional Description

4.3.1 Configuration register 1 (SYSCFG_CFG1)

Configure remapping of memory and DMA request.

Controlled specific I/O pin.

These two bytes are used to configure the storage type with the address of 0x0000 0000.

All of these bits can skip the hardware to have the software to select the physical mapping, and can be controlled and reset by software.

After reset, these bits select mode configuration parameters through BOOT pin.

Offset address: 0x00

Reset value: 0x0000 000X (X means memory mode, controlled by BOOT)

Field	Name	R/W	Description
1:0	MMSEL	R/W	Memory Mapping Select Control the memory mapping address 0x0000 0000. After reset, the parameters of these bits are determined by actual BOOT. X0: Main flash mapping address: 0x0000 0000 01: System flash mapping address: 0x0000 0000 11: Embedded SRAM mapping address: 0x0000 0000
7:2	Reserved		
8	ADCDMARMP	R/W	ADC DMA Request Remap Control remapping request of ADC DMA. 0: No remapping ADC—DMA_CH1 1: Remapping ADC—DMA_CH2
9	USART1TXRMP	R/W	USART1_TX DMA Request Remap This bit controls remapping request of USART1_TX DMA. 0: No remapping USART1_RX—DMA_CH2 1: Remapping USART1_RX—DMA_CH4
10	USART1RXRMP	R/W	USART1_RX DMA Request Remap This bit controls remapping request of USART1_RX DMA. 0: No remapping USART1_TX—DMA_CH3 1: Remapping USART1_TX—DMA_CH5
11	TMR16DMARMP	R/W	TMR16 DMA Request Remap This bit controls remapping request of TMR16 DMA. 0: No remapping TMR16_CH1 and TMR16_UP—DMA_CH3 1: Remapping TMR16_CH1 and TMR16_UP—DMA_CH4
12	TMR17DMARMP	R/W	TMR17 DMA Request Remap This bit control remapping request of TMR17. 0: No remapping TMR17_CH1 and TMR17_UP—DMA_CH1 1: Remapping TMR17_CH1 and TMR17_UP—DMA_CH2
15:13	Reserved		
16	I2CPB6FMP	R/W	Fast Mode Plus Driving Capability Activate for PB6 This bit enables PB6 interface to enable I2C fast mode plus. 0: PB6 pin is set as standard mode. 1: PB6 pin is set as I2C fast mode plus and I2C speed control is bypassed (ignored).
17	I2CPB7FMP	R/W	Fast Mode Plus Driving Capability Activate for PB7 This bit enables PB7 interface to enable I2C fast mode plus. 0: PB7 pin is set as standard mode. 1: PB7 pin is set as I2C fast mode plus and I2C speed control is bypassed (ignored).
18	I2CPB8FMP	R/W	Fast Mode Plus Driving Capability Activate for PB8 This bit enables PB8 interface to enable I2C fast mode plus. 0: PB8 pin is set as standard mode. 1: PB8 pin is set as I2C fast mode plus and I2C speed control is bypassed (ignored).
19	I2CPB9FMP	R/W	Fast Mode Plus Driving Capability Activate for PB9 This bit enables PB9 interface to enable I2C fast mode plus. 0: PB9 pin is set as standard mode. 1: PB9 pin is set as I2C fast mode plus and I2C speed control is bypassed (ignored).

Field	Name	R/W	Description
20	I2C1FMP	R/W	FM+ Driving Capability Activate for I2C1) 0: The fast mode plus is only controlled by I2CPxxFM+ bit. 1: All pins of I2C1 can be seleccted for fast mode plus by GPIO_AFx.
21	Reserved		
23:22	I2CFMP	R/W	Fast Mode Plus Driving Capability Activate for I2C PA9 and PA10 Enable the fast mode plus of PA9 and PA10 pins. 0: PAx pin is in standby mode. 1: Enabled and the speed control is bypassed(ignored)
31:24	Reserved		

4.3.2 External interrupt register 1 (SYSCFG_EINTCFG1)

These bits are controlled by software to be rewritten to select the external interrupt source of EINTx(x=0…3). The selected external interrupt sources represented by values of the EINTx [3:0] are shown in the table below.

Table 15 External Interrupt Sources Selected for Different Values

EINTx [3:0]	External interrupt source
x000	PA[x] pin
x001	PB[x] pin
x010	PC[x] pin
x011	PD[x] pin
x100	Reserved
x101	PF[x] pin
Others	Reserved

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	EINT0	R/W	EINT0 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT0. The selected external interrupt sources represented by values of the bits are shown in Table 15.
7:4	EINT1	R/W	EINT1 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT1. The selected external interrupt sources represented by values of the bits are shown in Table 15
11:8	EINT2	R/W	EINT2 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT2. The selected external interrupt sources represented by values of the bits are shown in Table 15

Field	Name	R/W	Description
15:12	EINT3	R/W	EINT3 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT3. The selected external interrupt sources represented by values of the bits are shown in Table 15
31:16	Reserved		

4.3.3 External interrupt register 2 (SYSCFG_EINTCFG2)

These bits are controlled by software to be rewritten to select the external interrupt source of EINTx(x=4…7). The selected external interrupt sources represented by values of the EINTx [3:0] are shown in Table 16.

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	EINT4	R/W	EINT4 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT4. The selected external interrupt sources represented by values of the bits are shown in Table 15
7:4	EINT5	R/W	EINT5 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT5. The selected external interrupt sources represented by values of the bits are shown in Table 15
11:8	EINT6	R/W	EINT6 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT6. The selected external interrupt sources represented by values of the bits are shown in Table 15
15:12	EINT7	R/W	EINT7 Configure) These bits are controlled by software to be rewritten to select the external interrupt source of EINT7. The selected external interrupt sources represented by values of the bits are shown in Table 15
31:16	Reserved		

4.3.4 External interrupt register 3 (SYSCFG_EINTCFG3)

These bits are controlled by software to be rewritten to select the external interrupt source of EINTx(x=8…11). The selected external interrupt sources represented by values of the EINTx [3:0] are shown in Table 16.

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	EINT8	R/W	EINT8 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT8. The selected external interrupt sources represented by values of the bits are shown in Table 15
7:4	EINT9	R/W	EINT9 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT9. The selected external interrupt sources represented by values of the bits are shown in Table15

Field	Name	R/W	Description
11:8	EINT10	R/W	EINT10 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT10. The selected external interrupt sources represented by values of the bits are shown in Table 15
15:12	EINT11	R/W	EINT11 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT11. The selected external interrupt sources represented by values of the bits are shown in Table 15
31:16	Reserved		

4.3.5 External interrupt register 4 (SYSCFG_EINTCFG4)

These bits are controlled by software to be rewritten to select the external interrupt source of EINTx(x=12 to 15). The selected external interrupt sources represented by values of the EINTx [3:0] are shown in Table 16.

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
3:0	EINT12	R/W	EINT12 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT12. The selected external interrupt sources represented by values of the bits are shown in Table 15.
7:4	EINT13	R/W	EINT13 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT13. The selected external interrupt sources represented by values of the bits are shown in Table 15.
11:8	EINT14	R/W	EINT14 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT14. The selected external interrupt sources represented by values of the bits are shown in Table 15.
15:12	EINT15	R/W	EINT15 Configure These bits are controlled by software to be rewritten to select the external interrupt source of EINT15. The selected external interrupt sources represented by values of the bits are shown in Table 15.
31:16	Reserved		

4.3.6 Configuration register 2 (SYSCFG_CFG2)

Offset address: 0x18

Reset value: 0x0000

Field	Name	R/W	Description
0	LOCK	R/W	Core LOCKUP Enable This bit is set by software and cleared by system reset. It can enable and lock the connection between Arm® Crotex®-M0+ LOCKUP Hardfault (hardware error) output and TMR1/15/16/17 break input. 0: Cortex®-M0+ LOCKUP output is disconnected from the TMR1/15/16/17 brake input 1: Cortex®-M0+ LOCKUP output is connected to the TMR1/15/16/17 brake input

Field	Name	R/W	Description
1	SRAMLOCK	R/W	SRAM Parity Check Lock This bit is set by software and is cleared by system reset. Can enable and lock the connection between SRAM parity error signal and TMR1/15/16/17 break input. 0: SRAM check error signal output is disconnected from the TMR1/15/16/17 brake input 1: SRAM check error signal output is connected to the TMR1/15/16/17 brake input
7:2	Reserved		
8	SRAMEFLG	RC_W1	SRAM Parity Error Flag When an SRAM parity error is detected, this bit will be set by hardware. This bit will be cleared when the software writes "1". 0: No SRAM parity check bit error is detected 1: SRAM parity check bit error
31:9	Reserved		

5 Reset and Clock Management (RCM)

5.1 Full Name and Abbreviation Description of Terms

Table 16 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Reset and Clock Management	RCM
Reset	RST
Power-On Reset	POR
Power-Down Reset	PDR
High Speed External Clock	HSECLK
Low Speed External Clock	LSECLK
High Speed Internal Clock	HSICLK
Low Speed Internal Clock	LSICLK
Phase Locked Loop	PLL
Main clock output	MCO
Calibrate	CAL
Trim	TRM
Wakeup	WUP
Automatic Wakeup	AWUP
Backup	BAKP
Low Power	LPWR
Clock Security System	CSS
Non Maskable Interrupt	NMI

5.2 Reset Functional Description

The supported reset is divided into three forms, namely, system reset, power reset and RTC area reset.

5.2.1 System Reset

5.2.1.1 "System reset" reset source

The reset source can be divided into external reset source and internal reset source.

External reset source:

- Low level on NRST pin

Internal reset source:

- Window watchdog termination count (WWDT reset)
- Independent watchdog termination count (IWDT reset)
- Software reset (SW reset)
- Low-power management reset
- Load option byte reset
- Power reset

A system reset will occur in case of any of the above events. Besides, the reset event source can be identified by viewing the reset flag bit in RCM_CSTS (control/state register).

Generally speaking, when the system is reset, the values of all registers except the reset flag bit of RCM_CSTS will be reset to the reset value.

Software reset

Software can be reset by putting SYSRESETREQ in Arm® Cortex®-M0+ interrupt application and reset control register to "1".

Low-power management reset

Low-power management may reset in two cases, one is when entering the standby mode, and the other is when entering the stop mode. In these two cases, if RSTSTDB bit (in standby mode) or RSTSTOP bit (in stop mode) in user selection byte is cleared, the system will be reset rather than entering the standby or stop mode.

For more information about user option bytes, refer to the chapter of "Flash memory".

Load option byte reset

The load byte reset is triggered by OBLOAD bit in FMC_CTRL2 register which is controlled by software.

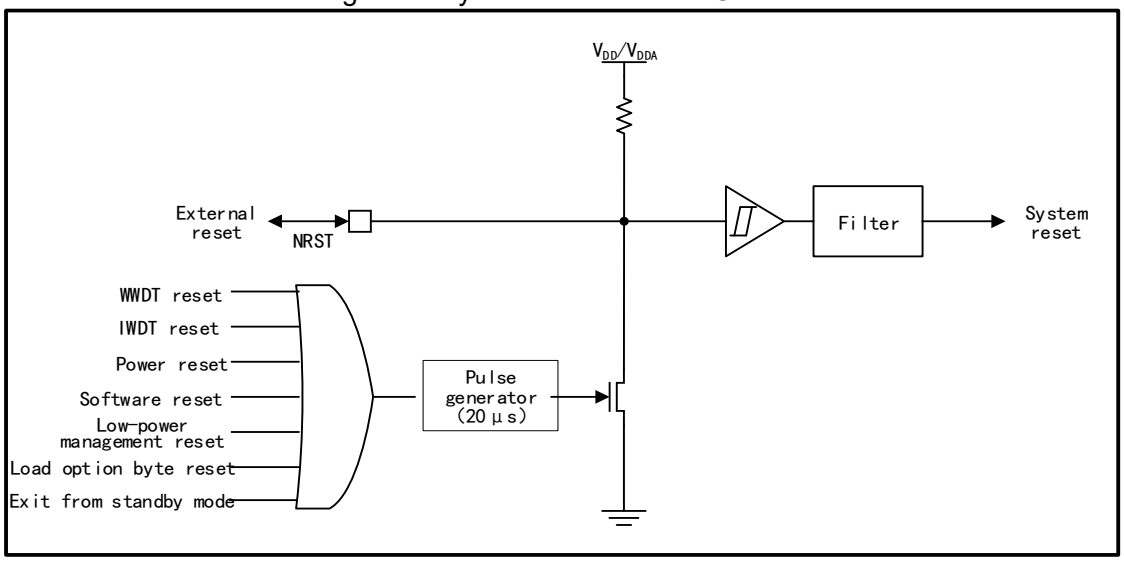
5.2.1.2 "System Reset" reset circuit

The reset source is used in the NRST pin, which remains low in reset process.

The internal reset source generates a delay of at least 60μs pulse on the NRST pin through the pulse generator, which causes the NRST to maintain the low level to generate reset; the external reset source directly pulls down the NRST pin level to generate reset.

The "system reset" reset circuit is shown in the figure below.

Figure 2 "System Reset" Reset Circuit



5.2.2 Power Reset

"Power reset" reset source

"Power reset" reset source is as follows:

- Power-on reset (POR reset)
- Power-down reset (PDR reset)
- Wake up from standby mode

A power reset will occur in case of any of the above events.

All registers will be reset by power reset.

5.2.3 RTC Domain Reset

"RTC domain reset" reset source

"RTC domain reset" reset source is as follows:

- Software reset triggered by resetting RTCRST bit in RCM_RTCCTRL
- Power-on reset (POR reset)

A RTC domain reset will occur in case of any of the above events.

RTC region reset only affects LSECLK oscillator, RTC real-time clock and register RCM_ RTCCTRL.

5.3 Functional Description of Clock Management

The clock sources of the whole system are: HSECLK, LSECLK, HSICLK, HSICLK14, LSICLK and PLL. For the characteristics of the clock source, please refer to the relevant chapter of "Electrical Characteristics" in the data manual.

5.3.1 External Clock Source

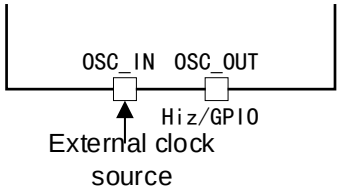
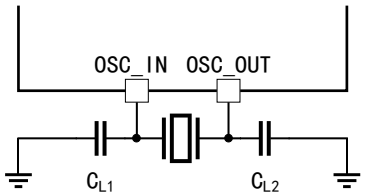
The external clock signal includes HSECLK (high-speed external clock signal) and LSECLK (low-speed external clock signal).

There are two kinds of external clock sources:

- External crystal/ceramic resonator
- External clock of user

The hardware configuration of the two kinds of clock sources is shown in the figure below.

Figure 3 HSECLK/LSECLK Clock Source Hardware Configuration

Clock source	Hardware configuration
External clock	
Crystal/ceramic resonator	

In order to reduce the distortion of clock output and shorten the start-up stabilization time, the crystal/ceramic resonator and load capacitor must be as close to the oscillator pin as possible.Adjust the value of load capacitance (C_{L1}, C_{L2}) according to the selected oscillator.

5.3.1.1 HSECLK high-speed external clock signal

HSECLK clock signal is generated by HSECLK external crystal/ceramic resonator and HSECLK external clock two kinds of clock sources.

Table 17 Clock Source Generting HSECLK

Name	Instruction
External clock source (HSECLK bypass)	Provide clock to MCU through OSC_IN pin. The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators; the waveform can be square wave, sine wave or triangle wave with 40%-60% duty cycle, and the maximum frequency is up to 32MHz. For hardware connection, it should be connected to OSC_IN pin, ensuring OSC_OUT pin is suspended; for MCU configuration, the user can select this mode by setting HSEBCFG and HSEEN bits in RCM_CTRL1 (clock control register 1).

Name	Instruction
External crystal/ceramic resonator (HSECLK crystal)	The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator. The frequency range is 4-32MHz. When needing to connect OSC_IN and OSC_OUT to the resonator, it can be enabled and disabled by setting the HSEEN bit in clock control register RCM_CTRL1 (clock control register). HSERDYFLG bit in the clock control register RCM_CTRL1 (clock control register 1) is used to indicate whether the high-speed external oscillator is stable. After startup, the clock is not released until this bit is set to "1" by hardware. If interrupt is allowed in RCM_INT (clock interrupt register), corresponding interrupt will be generated.

5.3.1.2 LSECLK low-speed external clock signal

LSECLK clock signal is generated by LSECLK external crystal/ceramic resonator and LSECLK external clock two kinds of clock sources.

Table 18 Clock Source Generting LSECLK

Name	Instruction
External clock source (LSECLK bypass)	The cock is provided to to MCU through OSC32_IN pin. The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators; the waveform can be square wave, sine wave or triangle wave with 50% duty cycle, and the signal frequency needs to be 32.768kHz. For hardware connection, it must be connected to OSC32_IN pin, ensuring OSC32_OUT pin is suspended; for MCU configuration, the user can select this mode by setting LSEBCFG and LSEEN bits in RCM_RTCCTRL.
External crystal/ceramic resonator (LSECLK crystal)	The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator. The frequency is 32.768kHz. OSC32_IN and OSC32_OUT needs to be connected to the oscillator which can be enabled and disabled through LSEEN bit in RCM_RTCCTRL. LSERDYFLG in RCM_RTCCTRL indicates whether LSECLK crystal oscillator is stable. At startup stage, LSECLK clock signal is not released until this bit is set to "1" by hardware. If it is allowed in the clock interrupt register, an interrupt request can be generated.

5.3.2 Internal Clock Source

The internal clock includes HSICLK (high-speed internal clock signal) and LSICLK (low-speed internal clock signal).

5.3.2.1 HSICLK high-speed internal clock signal

HSICLK clock signal is generated by internal 8MHz RC oscillator.

The RC oscillator frequency of different chips is different, and that of the same chip may be different with the change of temperature and voltage; the HSICLK clock frequency of each chip has been calibrated to 1% (25 ℃, V_{DD}=V_{DDA}=3.3V) by the manufacturer before leaving the factory. When the system is reset, the value calibrated by the manufacturer will be loaded to RCM_CTRL1 (clock control register); in addition, the users can further adjust the frequency by setting HSITRM in RCM_CTRL1 according to the application environment (temperature

and voltage) of the site.

HSIRDYFLG bit can be used to indicate whether HSICLK RC oscillator is stable. In the clock startup process, HSICLK RC output clock is not released until the HSIRDYFLG bit is set to "1" by hardware. HSICLK RC oscillator can be enabled or disabled by HSIEN bit in RCM_CTRL1.

Compared with HSECLK crystal oscillator, RC oscillator can provide system clock without any external device; the start time of RC oscillator is shorter than that of HSECLK crystal oscillator; even after calibration, its clock frequency accuracy is still inferior to that of HSECLK crystal oscillator.

5.3.2.2 LSICLK low-speed internal clock signal

Main characteristics of LSICLK

LSICLK is generated by RC oscillator, within the range of 40kHz (30kHz and 50kHz. The frequency may change along with the change of temperature and voltage. The clock can be provided to IWDT (independent watchdog) and RTC (real-time clcok) when keeping running in stop and standby mode.

LSICLK can be enabled or disabled by LSIEN bit of RCM_CSTS (control/state register). LSIRDYFLG bit in RCM_CSTS indicates whether the low-speed internal oscillator is stable. At startup stage, the clock is not released until this bit is set to "1" by hardware. If it is allowed in RCM_INT (clock interrupt register), LSICLK interrupt request will be generated.

5.3.3 PLL (Phase Locked Loop)

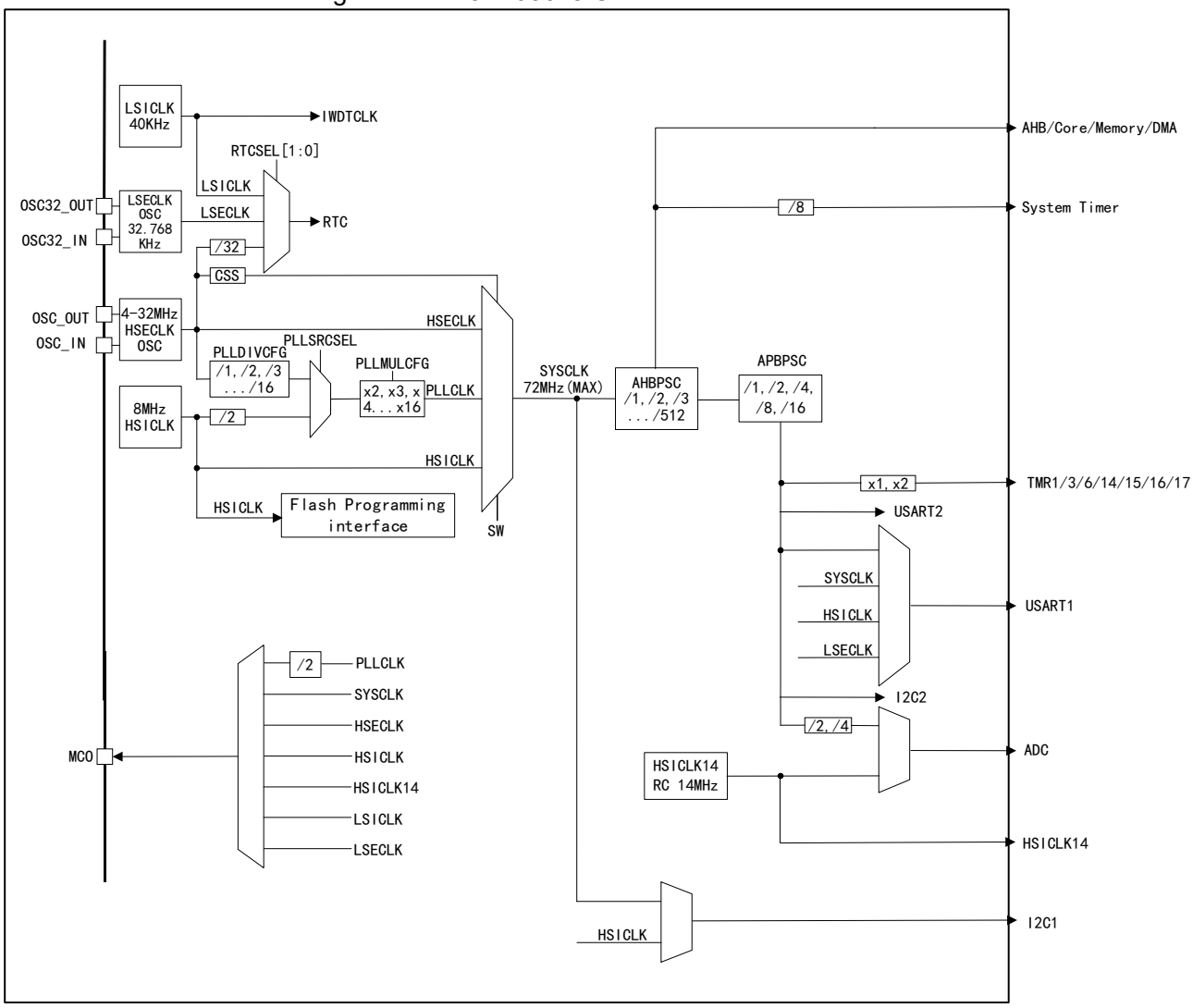
The main PLL can be used to double the frequency of HSICLK output clock or HSECLK crystal output clock.

To configure PLL parameters, first clear PLLEN bit, and after PLLRDYFLG is cleared (PLL is in the disabled state), change the parameters, then set PLLEN to 1, and by enabling PLL, when PLLRDYFLG is set to 1, the configuration is completed.The clock source and multiplication factor should be selected before being activated. Once PLL is activated, the selection cannot be changed.

When PLL is ready and PLL interrupt in RCM_INT is allowed, PLL can send interrupt request.

5.3.4 Clock Tree

Figure 4 APM32E030x8 Clock Tree



Note:

（1） HCLK means AHB clock.

（2） PCLK is clock signal of the peripheral connected to APB.

（3） FCLK is running clock of Arm® Cortex® -M0+.

（4） The frequency of AHB, APB can be configured through multiple prescalers

（5） When needing to run the peripheral connected to AHB and APB, it is required to turn on the corresponding enable end to make the peripheral get the clock signal.

（6） Frequency assignment of all TMRxCLK (timer clocks) is automatically set by the hardware according to the following two situations:

- If the corresponding APB prescaler factor is 1, the clock frequency of the timer is the same as that of the APB bus.
- Otherwise, the clock frequency of the timer will be set to twice the frequency of the APB bus connected to it.

（7） Moreover, the frequency of TMRx (x=1, 3, 6, 14, 15, 16, 17) clock signal is divided through APB.

5.3.5 Clock Source Selection of RTC

HSECLK/32, LSECLK or LSICLK can be selected as RTCCLK clock source by setting RTCSRCSEL bit in RCM_RTCCTRL. The selection of clock source can be changed only when the RTC domain is reset. Only when PCLK is greater than or equal to RTCCLK, can the system operate RTC normally.

5.3.6 Clock Source Selection of IWDT

When IWDT (independent watchdog) is opened, LSICLK oscillator will be opened by force, and when it is stable, the clock signal will be provided to IWDT. After LSICLK is opened by force, it will always be open and cannot be closed.

5.3.7 Clock Source Selection of MCO

When the corresponding GPIO port register is configured with corresponding function, the clock signal can be selected to be output to MCO pin by MCOSEL in configuration register RCM_CFG1 (clock configuration register). See the instructions for clock tree or MCOSEL bit of RCM_CFG1 register for specific clock signal.

5.3.8 Clock Source Selection of SYSCLK

SYSCLK clock source can be HSECLK, PLLCLK or HSICLK.

The state bit of RCM_CFG1 can indicate the ready clock and selected SYSCLK clock source.

When the system is reset, HSICLK oscillator is selected as the system clock, and the clock source cannot be stopped or by PLL is directly or indirectly used as the system clock. If you want to switch the SYSCLK clock source, you must wait until the destination clock source is ready (i.e. the destination clock source is stable).

5.3.9 CSS Clock Security System

In order to prevent MCU from normal operation due to external crystal oscillator short circuit, MCU can activate CSS clock security system through software. After the security system is activated, if the HSECLK oscillator is used as the system clock directly or indirectly (used as the PLL input clock and PLL is used as the system clock), the external HSECLK oscillator will be turned off when the HSECLK clock fails, and the system clock will automatically switch to HSICLK. At this time, the PLL which selects HSECLK as the clock input and as the system clock input source will also be turned off.

CSS can be activated by software. When HSECLK clock fails, CSS interrupt will be generated, and NMI will be generated automatically. NMI will be executed continuously until the CSS interrupt pending bit is cleared. Therefore, CSSCLR bit in RCM_INT (clock interrupt register) must be set in NMI processing program to clear the CSS interrupt.

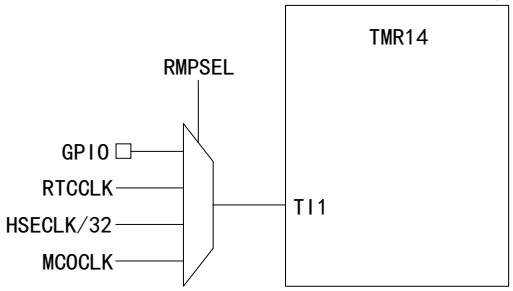
5.3.10 Clock Source Selection of ADC

The clock source of ADC is controlled through ADC_CFG2. It can select HSICLK14 or PCLK with the frequency divided by 2/4 as the clock source. When PCLK is used as the clock source of ADC, HSICLK14 cannot be changed over to ADC interface.

5.3.11 TMR14-based Internal/External Clock Measurement

Through the input capture function of TMR14 Channel 1, the frequency of all clock source generators on the motherboard can be indirectly measured. The circuit diagram is as follows:

Figure 5 TMR14 Indirect Measurement Clock Frequency Circuit Diagram



The input capture of TMR14 can select to connect the internal clock (RTCCLK, HSECLK/32, MCOCLK) of a GPIO port or a MCU by configuring RMPSEL bit of TMR14_OPT register of TMR14. See this register for specific configuration.

5.3.12 Low-power Mode

APB peripheral clock and DMA clock can be disabled by software.

Sleep mode:

- Stop CPU clock
- Flash and RAM interface clocks can be stopped by software
- When all peripheral clocks connected to APB bus are disabled, the hardware will stop the clocks of AHb1/APB bridge

Stop mode and standby mode:

- All 1.2V power domains are disabled
- PLLCLK, HSICLK, HSICLK14 and HSECLK are disabled

Deep sleep mode:

- The system can be debugged by setting the STOP_CLK_STS bit and STANDBY_CLK_STS bit in DBGMCU_CFG.
- The system selects HSICLK as SYSCLK through interrupt (in stop mode) or reset (standby mode)
- If Flash programming is in progress, the system will enter deep sleep mode only after all programming operations are completed
- If APB domain is being used, the system will enter deep sleep mode only after all operations are completed

5.4 Register Address Mapping

Table 19 RCM Register Address Mapping

Register name	Description	Offset address
RCM_CTRL1	Clock control register 1	0x00
RCM_CFG1	Clock configuration register 1	0x04
RCM_INT	Clock interrupt register	0x08
RCM_APBRST2	APB peripheral reset register 2	0x0C
RCM_APBRST1	APB peripheral reset register 1	0x10
RCM_AHBCLKEN	AHB peripheral clock enable register	0x14
RCM_APBCLKEN2	APB peripheral clock enable register 2	0x18
RCM_APBCLKEN1	APB peripheral clock enable register 1	0x1C
RCM_RTCCTRL	RTC domain control register	0x20

Register name	Description	Offset address
RCM_CSTS	Control/State register	0x24
RCM_IORST	I/O pin reset register	0x28
RCM_CFG2	Clock configuration register 2	0x2C
RCM_CFG3	Clock configuration register 3	0x30
RCM_CTRL2	Clock control register 2	0x34

5.5 Register Functional Description

5.5.1 Clock control register 1 (RCM_CTRL1)

Offset address: 0x00

Reset value: 0x0000 XX83; X means undefined

Access: Access in the form of word, half word and byte, without wait cycle

Field	Name	R/W	Description
0	HSIEN	R/W	High Speed Internal Clock Enable Set 1 or clear 0 by software. HSICLK is an RC oscillator. When one of the following conditions occurs, it will be set to 1 by the hardware: power-on start, software reset, wake-up from standby mode, wake-up from stop mode, failure of external high-speed clock source (as system clock or providing system clock through PLL). When HSICLK is used as system clock or provides system clock through PLL, this bit cannot be cleared. 0: HSICLK RC oscillator is disabled 1: HSICLK RC oscillator is turned on
1	HSIRDYFLG	R	High Speed Internal Clock Ready Flag 0: HSICLK RC oscillator is not stable 1: HSICLK RC oscillator is stable
2	Reserved		
7:3	HSITRM	R/W	High Speed Internal Clock Trim The product has been calibrated to 8MHz±1% when leaving the factory. However, it changes as the temperature and voltage changes, but the frequency of HSICLK RC oscillator can be adjusted by HSITRM[4:0]. For every 1Bit of value written, the frequency of HSICLK increases by about 40KHz.
15:8	HSICAL	R	High Speed Internal Clock Calibrate It will be calibrated to 8MHz±1% before leaving the factory. When the system is started up, the calibration parameters will be automatically written to the register.
16	HSEEN	R/W	High Speed External Clock Enable When entering the standby or stop mode, this bit is cleared by hardware and HSECLK is turned off; when HSECLK is used as system clock source or the system clock is provided through PLL, this bit cannot be cleared. 0: HSECLK is disabled 1: HSECLK is enabled
17	HSERDYFLG	R	High Speed External Clock Ready Flag When HSECLK is stable, this bit is set to 1 by hardware and cleared by software. 0: HSECLK is not stable 1: HSECLK is stable

Field	Name	R/W	Description
18	HSEBCFG	R/W	High Speed External Clock Bypass Configure Bypass mode refers to the mode in which external clock is used as the HSECLK clock source; otherwise the resonator is used as the HSECLK clock source. 0: Non-bypass mode 1: Bypass mode
19	CSSEN	R/W	Clock Security System Enable 0: Disable 1: Enable
23:20	Reserved		
24	PLLEN	R/W	PLL Enable When entering the standby and stop mode, this bit is cleared by the hardware; when PLLCLK has been configured (or in the process of configuration) as the clock source of the system clock, this bit cannot be cleared; in other cases, it cane set 1 or clear 0 by the software. 0: PLL is disabled 1: PLL is enabled
25	PLLRDYFLG	R	PLL Clock Ready Flag PLL is set to 1 by hardware after it is locked. 0: PLL is unlocked 1: PLL is locked
31:26	Reserved		

5.5.2 Clock configuration register 1 (RCM_CFG1)

Offset address: 0x04

Reset value: 0x0000 0000

All bits of this register are set or cleared by software.

Access: Access in the form of word, half word and byte, with 0 to 2 wait cycles. 1 or 2 wait cycles are inserted only when the access occurs during clock switching.

Field	Name	R/W	Description
1:0	SCLKSEL	R/W	System Clock Source Select When returning from stop or standby mode or the HSECLK directly or indirectly used as system clock fails, the hardware selects HSICLK as system clock by force (if the clock security system has been started) 00: HSICLK is used as system clock 01: HSECLK is used as system clock 10: PLLCLK is used as system clock 11: Reserved
3:2	SCLKSELSTS	R	System Clock Selection Status Indicate which clock source is used as system clock; set 1 or clear 0 by the hardware. 00: HSICLK is used as system clock 01: HSECLK is used as system clock 10: PLLCLK output is used as system clock 11: Unavailable
7:4	AHBPSC	R/W	AHB Clock Prescaler Factor Configure Control the prescaler factor of AHB clock. 0xxx: No frequency division for SYSCLK

Field	Name	R/W	Description
			1000: SYSCLK 2-divided frequency 1001: SYSCLK 4-divided frequency 1010: SYSCLK 8-divided frequency 1011: SYSCLK 16-divided frequency 1100: SYSCLK 64-divided frequency 1101: SYSCLK 128-divided frequency 1110: SYSCLK 256-divided frequency 1111: SYSCLK 512-divided frequency Note: When the prescaler factor of AHB clock is greater than 1, the prefetch buffer must be enabled.
10:8	APB1PSC	R/W	APB1 Clock Prescaler Factor Configure Control the prescaler factor of low-speed APB1 clock (PCLK1) 0xx: No frequency division for HCLK 100: HCLK 2-divided frequency 101: HCLK 4-divided frequency 110: HCLK 8-divided frequency 111: HCLK 16-divided frequency
15:11	Reserved		
16	PLLSRCSEL	R/W	PLL Clock Source Select This bit can be changed only when PLL is disabled. 0: HSICLK oscillator clock is used as the PLL input clock after 2 frequency division 1: HSECLK input clock as PLL
17	PLLHSEPSC	R/W	HSECLK Prescaler Factor for PLL Clock Source Refer to Bit 0 of RCM_CFG2.
21:18	PLLMULCFG	R/W	PLL Multiplication Factor Configure Determine PLL multiplication factor. This bit can be written only when PLL is disabled. 0000: PLLCLK 2-multiple frequency output 0001: PLL 3-multiple frequency output 0010: PLL 4-multiple frequency output 0011: PLL 5-multiple frequency output 0100: PLL 6-multiple frequency output 0101: PLL 7-multiple frequency output 0110: PLL 8-multiple frequency output 0111: PLL 9-multiple frequency output 1000: PLL 10-multiple frequency output 1001: PLL 11-multiple frequency output 1010: PLL 12-multiple frequency output 1011: PLL 13-multiple frequency output 1100: PLL 14-multiple frequency output 1101: PLL 15-multiple frequency output 1110: PLL 16-multiple frequency output 1111: PLL 16-multiple frequency output Note: The output frequency of PLL cannot be greater than 48MHz.

Field	Name	R/W	Description
23:22	Reserved		
27:24	MCOSEL	R/W	Main Clock Output Select Set or cleared by software. 0000: No clock output 0001: HSICLK14 is output as a clock 0010: LSICLK is output as a clock 0011: LSECLK is output as a clock 0100: SYSCLK is output as a clock 0101: HSICLK is output as a clock 0110: HSECLK is output as a clock 0111: PLLCLK is output as a clock 1xxx: Reserved
31:28	Reserved		

5.5.3 Clock interrupt register (RCM_INT)

Offset address: 0x08

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

Field	Name	R/W	Description
0	LSIRDYFLG	R	LSICLK Ready Interrupt Flag When LSICLK is stable and LSIRDYEN bit is set to 1, this bit will be set to 1 by hardware; when LSIRDYCLR is set to 1 by software, this bit will be cleared. 0: No LSICLK ready interrupt 1: LSICLK ready interrupt occurred
1	LSERDYFLG	R	LSECLK Ready Interrupt Flag When LSECLK is stable and LSERDYEN bit is set to 1, this bit will be set to 1 by hardware; when LSERDYCLR is set to 1 by software, this bit will be cleared. 0: No LSECLK ready interrupt 1: LSECLK ready interrupt occurred
2	HSIRDYFLG	R	HSICLK Ready Interrupt Flag When HSICLK is stable and HSIRDYEN bit is set to 1, this bit will be set to 1 by hardware; when HSIRDYCLR is set to 1 by software, this bit will be cleared. 0: No HSICLK ready interrupt 1: HSICLK ready interrupt occurred
3	HSERDYFLG	R	HSECLK Ready Interrupt Flag When HSECLK is stable and HSERDYEN bit is set to 1, this bit will be set to 1 by hardware; when HSERDYCLR is set to 1 by software, this bit will be cleared. 0: No HSECLK ready interrupt 1: HSECLK ready interrupt occurred
4	PLLRDYFLG	R	PLL Ready Interrupt Flag When PLL is stable and PLLRDYEN bit is set to 1, this bit will be set to 1 by hardware; when PLLRDYCLR is set to 1 by software, this bit will be cleared. 0: No clock ready interrupt caused by PLL locked 1: Clock ready interrupt caused by PLL locked
5	HSI14RDYFLG	R	HSICLK14 Ready Interrupt Flag When the internal high-speed clock is ready and the HSI14RDYEN bit is set to 1, it is set to 1 by hardware. When HSI14RDYCLR is set to 1 by software, this bit will be cleared. 0: No security system interrupt caused by HSI14CLK failure 1: Security system interrupt is caused by HSI14CLK failure

Field	Name	R/W	Description
6	Reserved		
7	CSSFLG	R	Clock Security System Interrupt Flag When the external 4-16MHz oscillator clock fails, it is set to 1 by hardware. When CSSCLR is set to 1 by software, this bit will be cleared. 0: No security system interrupt caused by HSE clock failure 1: Clock security system interrupt is caused by HSE clock failure
8	LSIRDYEN	R/W	LSICLK Ready Interrupt Enable Enable or disable internal 40kHz RC oscillator ready interrupt. 0: Disable 1: Enable
9	LSERDYEN	R/W	LSECLK Ready Interrupt Enable Enable external 32kHz RC oscillator ready interrupt. 0: Disable 1: Enable
10	HSIRDYEN	R/W	HSICLK Ready Interrupt Enable Enable the internal 8MHz RC oscillator ready interrupt. 0: Disable 1: Enabled
11	HSERDYEN	R/W	HSCLKE Ready Interrupt Enable Enable external 4-16MHz oscillator ready interrupt. 0: Disable 1: Enable
12	PLLRDYEN	R/W	PLL Ready Interrupt Enable Enable PLL ready interrupt. 0: Disable 1: Enable
13	HSI14RDYEN	R/W	HSICLK14 Ready Interrupt Enable Enable the internal 14MHz RC oscillator ready interrupt. 0: Disable 1: Enable
15:14	Reserved		
16	LSIRDYCLR	W	LSICLK Ready Interrupt Clear Clear LSI ready interrupt flag bit LSIRDYFLG. 0: No effect 1: Clear
17	LSERDYCLR	W	LSECLK Ready Interrupt Clear Clear LSE ready interrupt flag bit LSERDYFLG. 0: No effect 1: Clear
18	HSIRDYCLR	W	HSICLK Ready Interrupt Clear Clear HSICLK ready interrupt flag bit HSIRDYFLG. 0: No effect 1: Clear
19	HSERDYCLR	W	HSECLK Ready Interrupt Clear Clear HSECLK ready interrupt flag bit HSERDYFLG. 0: No effect 1: Clear
20	PLLRDYCLR	W	PLL Ready Interrupt Clear Clear PLL ready interrupt flag bit PLLRDYFLG. 0: No effect 1: Clear
21	HSI14RDYCLR	W	HSICLK14 Ready Interrupt Clear Clear the ready interrupt flag bit HSI14RDYFLG of HSICLK14. 0: No effect 1: Clear
22	Reserved		
23	CSSCLR	W	Clock Security System Interrupt Clear Clear the security system interrupt flag bit CSSFLG. 0: No effect 1: Clear

Field	Name	R/W	Description
31:24	Reserved		

5.5.4 APB peripheral reset register 2 (RCM_APBRST2)

Offset address: 0x0C

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle.

All bits can be reset or cleared by software.

Field	Name	R/W	Description
0	SYSCFGRST	R/W	SYSCFG Reset 0: No effect 1: Reset
8:1	Reserved		
9	ADCRST	R/W	ADC Reset 0: No effect 1: Reset
10	Reserved		
11	TMR1RST	R/W	TMR1 Timer Reset 0: No effect 1: Reset
12	SPI1RST	R/W	SPI1 Reset 0: No effect 1: Reset
13	Reserved		
14	USART1RST	R/W	USART1 Reset 0: No effect 1: Reset
15	Reserved		
16	TMR15RST	R/W	TMR15 Reset 0: No effect 1: Reset
17	TMR16RST	R/W	TMR16 Reset 0: No effect 1: Reset
18	TMR17RST	R/W	TMR17 Reset 0: No effect 1: Reset
21:19	Reserved		
22	DBGRST	R/W	Debug Reset 0: No effect 1: Reset
31:23	Reserved		

5.5.5 APB peripheral reset register 1 (RCM_APBRST1)

Offset address: 0x10

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle

Field	Name	R/W	Description
0	Reserved		
1	TMR3RST	R/W	Timer 3 Reset 0: No effect 1: Reset
3:2	Reserved		
4	TMR6RST	R/W	Timer 6 Reset 0: No effect 1: Reset
7:5	Reserved		
8	TMR14RST	R/W	Timer 14 Reset 0: No effect 1: Reset
10:9	Reserved		
11	WWDTRST	R/W	Window Watchdog Reset 0: No effect 1: Reset
13:12	Reserved		
14	SPI2RST	R/W	SPI2 Reset 0: No effect 1: Reset
16:15	Reserved		
17	USART2RST	R/W	USART2 Reset 0: No effect 1: Reset
20:18	Reserved		
21	I2C1RST	R/W	I2C1 Reset 0: No effect 1: Reset
22	I2C2RST	R/W	I2C2 Reset 0: No effect 1: Reset
27:23	Reserved		
28	PMURST	R/W	Power Interface Reset 0: No effect 1: Reset
31:29	Reserved		

5.5.6 AHB peripheral clock enable register (RCM_AHBCLKEN)

Offset address: 0x14

Reset value: 0x0000 0014

Access: Access in the form of word, half word and byte, without wait cycle

All bits can be reset or cleared by software.

Note: When the peripheral clock is not enabled, the software cannot read the value of the peripheral register, and the value returned is always 0x0.

Field	Name	R/W	Description
0	DMAEN	R/W	DMA Clock Enable 0: Disable 1: Enable
1	Reserved		
2	SRAMEN	R/W	SRAM Interface Clock Enable Enable SRAM clock in sleep mode. 0: Disable 1: Enable
3	Reserved		
4	FMCEN	R/W	FMC Clock Enable Enable the flash interface circuit clock in sleep mode. 0: Disable 1: Enable
5	Reserved		
6	CRCEN	R/W	CRC Clock Enable 0: Disable 1: Enable
16:7	Reserved		
17	PAEN	R/W	I/O PortA Clock Enable 0: Disable 1: Enable
18	PBEN	R/W	I/O PortB Clock Enable 0: Disable 1: Enable
19	PCEN	R/W	I/O PortC Clock Enable 0: Disable 1: Enable
20	PDEN	R/W	I/O PortD Clock Enable 0: Disable 1: Enable
21	Reserved		
22	PFEN	R/W	I/O PortF Clock Enable 0: Disable 1: Enable
31:23	Reserved		

5.5.7 APB peripheral clock enable register 2 (RCM_APBCLKEN2)

Offset address: 0x18

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte

Usually there is no wait cycle. However, when the peripheral on the APB2 bus is accessed, the waiting state will be inserted until the APB2 peripheral access ends.

All bits can be reset or cleared by software.

Note: When the peripheral clock is not enabled, the software cannot read the value of the peripheral register, and the value returned is always 0x0.

Field	Name	R/W	Description
0	SYSCFGEN	R/W	SYSCFG Clock Enable 0: Disable 1: Enable
4:1	Reserved		
5	USART6EN	R/W	USART6 Clock Enable 0: Disable 1: Enable
8:6	Reserved		
9	ADCEN	R/W	ADC Interface Clock Enable 0: Disable 1: Enable
10	Reserved		
11	TMR1EN	R/W	TMR1 Timer Clock Enable 0: Disable 1: Enable
12	SPI1EN	R/W	SPI 1 Clock Enable 0: Disable 1: Enable
13	Reserved		
14	USART1EN	R/W	USART1 Clock Enable 0: Disable 1: Enable
15	Reserved		
16	TMR15EN	R/W	TMR15 Timer Clock Enable 0: Disabled 1: Enabled
17	TMR16EN	R/W	TMR16 Timer Clock Enable 0: Disable 1: Enable
18	TMR17EN	R/W	TMR17 Timer Clock Enable 0: Disable 1: Enable
21:19	Reserved		

Field	Name	R/W	Description
22	DBGEN	R/W	Debug Clock Enable 0: Disable 1: Enable
31:23	Reserved		

5.5.8 APB peripheral clock enable register 1 (RCM_APBCLKEN1)

Offset address: 0x1C

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte

Usually there is no wait cycle. However, when the peripheral on the APB bus is accessed, the waiting state will be inserted until the APB peripheral access ends.

All bits can be reset or cleared by software.

Note: When the peripheral clock is not enabled, the software cannot read the value of the peripheral register, and the value returned is always 0x0.

Field	Name	R/W	Description
0	Reserved		
1	TMR3EN	R/W	Timer 3 Clock Enable 0: Disable 1: Enable
3:2	Reserved		
4	TMR6EN	R/W	Timer 6 Clock Enable 0: Disable 1: Enable
7:5	Reserved		
8	TMR14EN	R/W	Timer 14 Clock Enable 0: Disable 1: Enable
10:9	Reserved		
11	WWDTEN	R/W	Window Watchdog Clock Enable 0: Disable 1: Enable
13:12	Reserved		
14	SPI2EN	R/W	SPI 2 Clock Enable 0: Disable 1: Enable
16:15	Reserved		
17	USART2EN	R/W	USART 2 Clock Enable 0: Disable 1: Enable
20:18	Reserved		

Field	Name	R/W	Description
21	I2C1EN	R/W	I2C1 Clock Enable 0: Disable 1: Enable
22	I2C2EN	R/W	I2C2 Clock Enable 0: Disable 1: Enable
27:23	Reserved		
28	PMUEN	R/W	Power Interface Clock Enable 0: Disable 1: Enable
31:29	Reserved		

5.5.9 RTC domain control register (RCM_RTCCTRL)

Offset address: 0x20

Reset value: 0x0000 0018, which can be reset effectively only by RTC domain

Access: Access in the form of word, half word and byte, with 0 to three wait cycles

When the register is accessed continuously, the waiting state will be inserted.

Note: Only when BPWEN bit in PMU_CTRL is set to 1, can LSEEN, LSEBCFG, RTCSRCSEL and RTCCLKEN be changed.

Field	Name	R/W	Description
0	LSEEN	R/W	Low-Speed External Oscillator Enable 0: Disable 1: Enable
1	LSERDYFLG	R	Low-Speed External Clock Ready Flag When LSECLK is stable, this bit is set to 1 by hardware, and when it is unstable, it is cleared by hardware. 0: Not ready 1. Ready
2	LSEBCFG	R/W	Low-Speed External Clock Bypass Mode Configure Bypass mode refers to the mode in which external clock is used as the LSECLK clock source; otherwise the resonator is used as the LSECLK clock source. 0: Non-bypass mode 1: Bypass mode
4:3	LSEDRVCFG	R/W	LSE Oscillator Drive Capability Configure This bit is set or cleared by software; set the driving capability of LSECLK oscillator (crystal mode is not bypassed). When the RTC domain is reset, this bit is restored to the default value. 00: Weak 01: Medium and low 10: Medium and high 11: Strong
7:5	Reserved		

Field	Name	R/W	Description
9:8	RTCSRCSEL	R/W	RTC Clock Source Select First set the RTCRST bit to reset the RTC domain, and then select the RTC clock source. It is impossible to directly configure the register to modify. 00: No clock 01: LSECLK is used as RTC clock 10: LSICLK is used as RTC clock 11: HSECLK is used as RTC clock after 32 divided frequency
14:10	Reserved		
15	RTCCLKEN	R/W	RTC Clock Enable 0: Disable 1: Enable
16	RTCRST	R/W	RTC Domain Software Reset Set 1 or clear 0 by software 0: Reset is not activated 1: Reset RTC domain (only affecting LSECLK oscillator, RTC clock and register RCM_RTCCTRL)
31:17	Reserved		

5.5.10 Control/State register (RCM_CSTS)

Offset address: 0x24

Reset value: 0xXXX0 0000, except reset flag, all are cleared by system reset, and reset flag can only be cleared by power reset.

Access: Access in the form of word, half word and byte, with 0 to three wait cycles.

When the register is accessed continuously, the waiting state will be inserted.

Field	Name	R/W	Description
0	LSIEN	R/W	Low-Speed Internal Oscillator Enable Set 1 or clear 0 by software. 0: Disable 1: Enable
1	LSIRDYFLG	R	Low-Speed Internal Oscillator Ready Flag When LSICLK is stable, this bit is set to 1 by hardware, and when it is unstable, it is cleared by hardware. 0: Not ready 1. Ready
22:2	Reserved		
23	PWRRSTFLG	R	Reset Flag of The 1.2V Domain When a reset occurs in the 1.2V power domain, the hardware is set to 1 by clearing the RSTFLGCLR set. 0: reset does not occur 1: Reset occurs
24	RSTFLGCLR	RT_W	Reset Flag Clear The reset flag is set or cleared by software, including RSTFLGCLR.

Field	Name	R/W	Description
			0: No effect 1: Clear the reset flag
25	OBRSTFLG	R	Option Byte Loader Reset Flag When the option byte load reset occurs, it is set by hardware; otherwise, it is set and cleared by RSTFLGCLR. 0: Reset does did not occur 1: Reset occurred
26	PINRSTFLG	R	NRST PIN Reset Occur Flag When the NRST pin reset occurs, it is set to 1 by the hardware; Cleared by the software by writing the RSTFLGCLR bit. 0: No NRST pin reset occurs 1: An NRST pin reset occurs
27	PODRSTFLG	R	POR/PDR Reset Occur Flag Set 1 by hardware; clear 0 by software by writing RSTFLGCLR bit. 0: No power-on/power-down reset occurs 1: Power-on/power-down reset occurs
28	SWRSTFLG	R	Software Reset Occur Flag Set 1 by hardware; clear 0 by software by writing RSTFLGCLR bit. 0: Not occur 1: Occurred
29	IWDTRSTFLG	R	Independent Watchdog Reset Occur Flag When independent watchdog reset occurs in V_{DD} area, it is set to 1 by hardware and cleared by software by writing RSTFLGCLR bit. 0: Not occur 1: Occurred
30	WWDTRSTFLG	R	Window Watchdog Reset Occur Flag When window watchdog is reset, it is set to 1 by hardware and cleared by software by writing RSTFLGCLR bit. 0: Not occur 1: Occurred
31	LPWRRSTFLG	R	Low Power Reset Occur Flag When low-power management is reset, it is set to 1 by hardware and cleared by software by writing RSTFLGCLR bit. 0: Not occur 1: Occurred

5.5.11 AHB peripheral reset register (RCM_ AHBRST)

Offset address: 0x28

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle

Set 1 or clear 0 by software.

Field	Name	R/W	Description
16:0	Reserved		

Field	Name	R/W	Description
17	PARST	R/W	I/O Port A Reset 0: Invalid 1: Reset
18	PBRST	R/W	I/O Port B Reset 0: Invalid 1: Reset
19	PCRST	R/W	I/O Port C Reset 0: Invalid 1: Reset
20	PDRST	R/W	I/O Port D Reset 0: Invalid 1: Reset
21	Reserved		
22	PFRST	R/W	I/O Port F Reset 0: Invalid 1: Reset
31:23	Reserved		

5.5.12 Clock configuration register 2 (RCM_CFG2)

Offset address: 0x2C

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle

Field	Name	R/W	Description
3:0	PLLDIVCFG	R/W	PLLCLK Input Division Factor Configure Configure the input clock signal division factor of PLLCLK. 0000: No frequency of division 0001: 2 divided frequency 0010: 3 divided frequency 0011: 4 divided frequency .... 1101: 14 divided frequency 1110: 15 divided frequency 1111: 16 divided frequency
31:4	Reserved		

5.5.13 Clock configuration register 3 (RCM_CFG3)

Offset address: 0x30

Reset value: 0x0000 0000

Access: Access in the form of word, half word and byte, without wait cycle

Field	Name	R/W	Description
1:0	USART1SEL	R/W	USRAT1 Clock Source Select Set or cleared by software. The default value is 00. 00: PCLK is used as USART1CLK 01: SYSCLK is used as USART1CLK 10: LSECLK is used as USART1CLK 11: HSICLK is used as USART1CLK

Field	Name	R/W	Description
3:2	Reserved		
4	I2C1SEL	R/W	I2C1 Clock Source Select Set or cleared by software. The default value is 0. 0: HSICLK is used as I2C1CLK 1: SYSCLK is used as I2C1CLK
31:5	Reserved		

5.5.14 Clock control register 2 (RCM_CTRL2)

Offset address: 0x34

Reset value: 0xXX00 XX80; X means undefined

Access: Access in the form of word, half word and byte, without wait cycle

Field	Name	R/W	Description
0	HSI14EN	R/W	HSICLK14 Enable Set 1 or clear 0 by software. 0: Internal 14MHz oscillator OFF 1: Internal 14MHz oscillator ON
1	HSI14RDFLG	R	HSICLK14 Ready Flag This bit is set by hardware to indicate the state of HSICLK14 oscillator. 0: Not ready 1: Ready
2	HSI14TO	R/W	ADC Interface Turn On HSICLK14 ADC interface can turn on HSICLK14 oscillator, which is set or cleared by hardware. 0: Can be turned on 1: Cannot be turned on
7:3	HSI14TRM	R/W	HSICLK14 Trim The product has been calibrated to 14MHz±1% when leaving the factory. However, it changes as the temperature and voltage changes, but the frequency of HSICLK14 RC oscillator can be adjusted by HSI14TRM.
15:8	HSI14CAL	R	HSICLK14 Calibrate It will be calibrated to 14MHz±1% before leaving the factory. When the system is started up, the calibration parameters will be automatically written to the register.
31:16	Reserved		

6 Power Management Unit (PMU)

6.1 Full Name and Abbreviation Description of Terms

Table 20 Full Name and Abbreviation Description of Terms

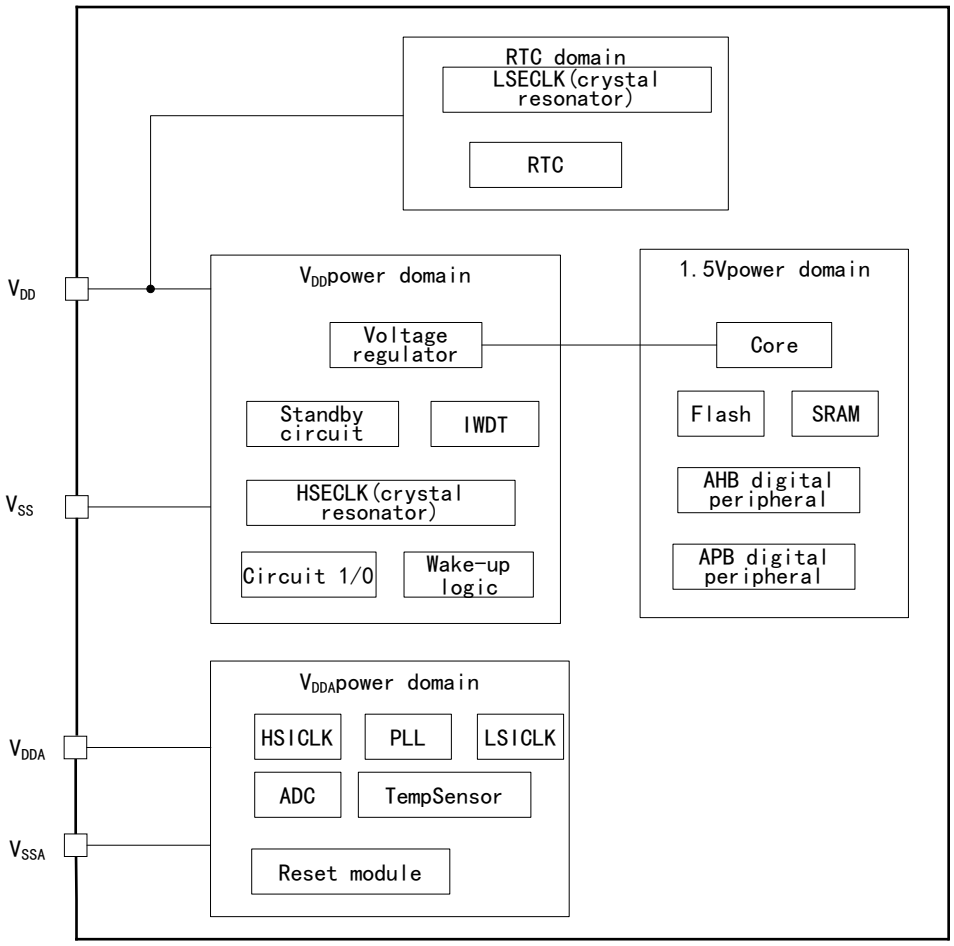
Full name in English	English abbreviation
Power Management Unit	PMU
Power On Reset	POR
Power Down Reset	PDR
Power Voltage Detector	PVD

6.2 Introduction

The power supply is the foundation for stable operation of a system, with working voltage of 2.0 ~ 3.6V, and 1.2V power supply can be provided through the built-in voltage regulator.

6.3 Structure Block Diagram

Figure 6 Power Supply Control Structure Block Diagram



6.4 Functional Description

6.4.1 Power Domain

The power domain of the product includes: V_{DD} power domain, V_{DDA} power domain, and 1.5V power domain.

6.4.1.1 V_{DD} Power Domain

Power supply is provided through V_{DD}/V_{SS} pins to power the voltage regulator, standby circuit, IWDT, HSECLK, I/O (except PC13, PC14, PC15 pins) and wake-up logic.

Voltage regulator

Power can be supplied to 1.5V power domain in the following operating modes:

- Normal mode: In this mode, 1.5V power supply area runs at full power
- Stop mode: In this mode, 1.5V power supply area works in low power state, all clocks are off, and peripherals stop work

- Standby mode: In this mode, the 1.5V power supply area stops power supply, and except for the standby circuit, the content of register and SRAM will be lost

6.4.1.2 V_{DDA} power domain

Power the ADC, HSICLK, LSICLK, TempSensor, PLL and reset module through V_{DDA}/V_{SSA} pins.

Independent ADC power supply

Independent ADC power supply can improve conversion accuracy, and the specific power pins are as follows:

- V_{DDA}: Power pin of ADC
- V_{SSA}: Independent power ground pin

6.4.1.3 1.5V power domain

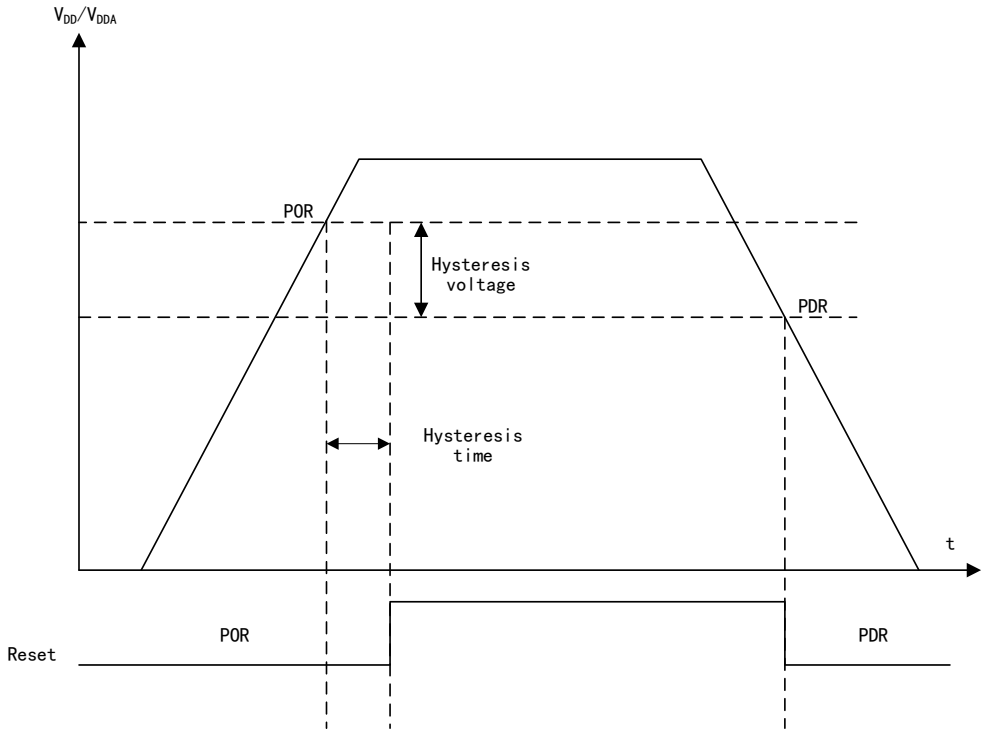
The core, Flash, SRAM and digital peripherals are powered by voltage regulator.

6.4.2 Power Management

6.4.2.1 Power-on/power-down reset (POR and PDR)

When the V_{DD}/V_{DDA} is detected to be lower than the threshold voltage VPOR and VPDR, the chip will automatically maintain the reset state. The waveform diagrams of power-on reset and power-down reset are as follows. For POR, PDR, hysteresis voltage and hysteresis time, please refer to the "Datasheet".

Figure 7 Power-on Reset and Power-down Reset Oscillogram



6.4.3 Power Consumption Control

6.4.3.1 Reduce the power consumption in low-power mode

There are three low-power modes: sleep mode, stop mode and standby mode. The power consumption is reduced by closing the core and clock source and setting the voltage regulator.

The power consumption, wake-up start time, wake-up mode and data storage of each low-power mode are different; the lower the power consumption is, the longer the wake-up time is, the less the wake-up mode is, the less the data saved are after wake-up; users can choose the most appropriate low-power mode according to their needs. The following table shows the difference among three low-power modes.

Table 21 Difference among "Sleep Mode, Stop Mode and Standby Mode"

Mode	Instruction	Entry mode	Wake-up mode	Voltage regulator	Effect on 1.5V area clock	Effect on V_{DD} area clock
Sleep	Arm® Cortex®-M0+ core stops, and all peripherals including the core peripheral are still working	Call WFI instruction	Any interrupt	Open	Ony the core clock is turned off and it has no effect on other clocks and ADC clocks	None
		Call WFE instruction	Wake-up event	Open		None
Stop	All clocks have stopped	PDDSCFG and LPDSCFG bits +SLEEPDEEP bit +WFI or WFE	Anny external interrupt	Turn on or be in low-power mode	Close clocks of all 1.2V areas	The oscillator of HSICLK and HSECLK is turned off
Standby	1.2V power off	PDDSCFG bit +SLEEPDEEP bit +WFI or WFE	Rising edge of WKUP pin, RTC alarm event, external reset on NRST pin, IWDT reset	Off		

Sleep mode

The characteristics of sleep mode are shown in the table below

Table 22 Characteristics of Sleep Mode

Characteristics	Instruction
Enter	Execute WFI or WFE instructions when kernel register SLEEPDEEP=0: When SLEEPONEXIT is set to 0, it enters sleep mode immediately. when SLEEPONEXIT is set to 1, the system will exit the interrupt program and then enter the sleep mode immediately.
Wake-up	If WFI instruction is executed to enter the sleep mode, wake up by any interrupt; If WFE instruction is executed to enter the sleep mode, wake up through an event.
Sleep	The core stops working, all peripherals are still running, and the data in the core registers and memory before sleep are saved.
Wake-up delay	None
After wake-up	If the system is woken up by interrupt, it will first enter the interrupt, then exit the interrupt, and then execute the program after WFI instruction. If the system is woken up by event, it will directly execute the program after WFE instruction.

Stop mode

The characteristics of stop mode are shown in the table below:

Table 23 Characteristics of Stop Mode

Characteristics	Instruction
Enter	SLEEPDEEP bit of the core register is set to 1, PDDSCFG bit of the register PMU_CTRL is set to 0, and when executing WFI or WFE instruction, the system will enter the stop mode immediately; When LPDSCFG bit of the register PMU_CTRL is set to 0, the voltage regulator is working in normal mode; when LPDSCFG bit of the register PMU_CTRL is set to 1, the voltage regulator is working in low-power mode.
Wake-up	If WFI instruction is executed to enter the sleep mode, wake up by any interrupt; If WFE instruction is executed to enter the sleep mode, wake up through an event.
Stop	The core will stop working, the peripheral will stop working, and the data in the core register and memory before stop will be saved.
Wake-up delay	HSICLK oscillator wake-up time + voltage regulator wake-up time from low-power mode.
After wake-up	If the system is woken up by interrupt, it will first enter the interrupt, then exit the interrupt, and then execute the program after WFI instruction. If the system is woken up by event, it will directly execute the program after WFE instruction.

Standby mode

The characteristics of standby mode are shown in the table below:

Table 24 Standby Mode

Characteristics	Instruction
Enter	SLEEPDEEP bit of the core register is set to 1, PDDSCFG bit of the register PMU_CTRL is set to 1, WUEFLG bit is set to 0 and when executing WFI or WFE instruction, the system will enter the standby mode immediately.
Wake-up	Wake up by rising edge of WKUP pin, RTC alarm, wake-up, tamper, timestamp event or NRST pin external reset and IWDT reset.
Standby	The core will stop working, the peripheral will stop working, and the data in the core register and memory will be lost.
Wake-up delay	Chip reset time.
After wake-up	The program starts executing from the beginning.

6.4.3.2 Reduce the power consumption in run mode

In the run mode, the power consumption can be reduced by reducing the system clock, closing or reducing the peripheral clock on the APB/AHB bus.

6.5 Register Address Mapping

Table 25 PMU Register Address Mapping Table

Register name	Description	Offset address
PMU_CTRL	Power control register	0x00
PMU_CSTS	Power control/state register	0x04

6.6 Register Functional Description

6.6.1 Power control register (PMU_CTRL)

Offset address: 0x00

Reset value: 0x0000 0000 (cleared when waking up from standby mode)

Field	Name	R/W	Description
0	LPDSCFG	R/W	Low-power deep sleep configuration (Low Power Deepsleep Configure) Configure the working state of the voltage regulator in stop mode. 0: Enable 1: Low-power mode
1	PDDSCFG	R/W	Configure the power-down deep sleep (Power Down Deep Sleep Configure) When the CPU enters deep sleep, configure the voltage regulator state in standby and stop modes. 0: The voltage regulator is controlled by LPDSCFG bit when entering the stop mode 1: Enter standby mode
2	WUFLGCLR	RC_W1	Clear the wakeup flag (Wakeup Flag Clear) 0: Invalid 1: Clear the wake-up flag after 2 system clock cycles by writing 1
3	SBFLGCLR	RC_W1	Clear the standby flag (Standby Flag Clear) 0: Invalid 1: Write 1 to clear the standby flag
7:4	Reserved		
8	BPWEN	R/W	Enable the write RTC area (RTC Domain Write Access Enable) RTC area refers to RTC and RTC register; write access is disabled after reset, and is allowed after writing 1. 0: Write is disabed 1: Write is enabled
31:9	Reserved		

6.6.2 Power control/state register (PMU_CSTS)

Offset address: 0x04

Reset value: 0x0000 000X (not cleared when waking up from standby mode)

Compared with the standard APB read, it requires extra APB cycle to read this register

Field	Name	R/W	Description
0	WUEFLG	R	Wakeup Event Flag This bit is set by hardware, indicating whether wake-up event or RTC alarm wake-up event occurs on WKUP pin. 0: Not occur 1: Occurred Note: Enable the WKUP pin, and an event will be detected when the WKUP pin is at high level.
1	SBFLG	R	Standby Flag This bit is set to 1 by hardware, and can only be cleared by POR/PDR (power-on/power-down reset) or by setting the SBFLGCLR bit of the power supply control register (PMU_CTRL). 0: Not enter the standby mode 1: Have entered the standby mode
7:2	Reserved		

Field	Name	R/W	Description
9:8	WKUPCFGx	R/W	WKUPxPin Configure When WKUPx is used as a normal I/O, the event on WKUPx pin cannot wake up the CPU in standby mode; it can wake up CPU only when it is not used as a normal I/O. 0: Configure normal I/O 1: Can wake MCU Note: Clear this bit in system reset.
31:10	Reserved		

7 Nested Vector Interrupt Controller (NVIC)

7.1 Full Name and Abbreviation Description of Terms

Table 26 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Non Maskable Interrupt	NMI

7.2 Introduction

The Cortex-M0+ core in the product integrates nested vectored interrupt controller (NVIC), which is closely coupled with the core, and can handle exceptions and interrupts and power management control efficiently and with low delay. Please see *Cortex-M0+ Technical Reference Manual* for more instructions about NVIC.

7.3 Main Characteristics

（1） 32 maskable interrupt channels (excluding 16 Cortex-M0+ interrupt lines)

（2） 4 programmable priority levels (use 2-bit interrupt priority level)

（3） Low-delay exception and interrupt processing

（4） Power management control

（5） Realization of system control register

7.4 Interrupt and Exception Vector Table

Table 27 Interrupt and Exception Vector Table

Name	Vector No.	Priority	Vector address	Description
-	-	-	0x0000_0000	Reserved
RST	-	-3	0x0000_0004	Reset
NMI	-	-2	0x0000_0008	Non-maskable interrupt
Hardware fault	-	-1	0x0000_000C	Various hardware faults
SVCall	-	Can be set	0x0000_002C	System service called by SWI instruction
PendSV	-	Can be set	0x0000_0038	Pending system service
SysTick	-	Can be set	0x0000_003C	System tick timer
WWDT	0	Can be set	0x0000_0040	Window watchdog interrupt
-	1	-	0x0000_0044	Reserved
RTC	2	Can be set	0x0000_0048	RTC interrupt

Name	Vector No.	Priority	Vector address	Description
FLASH	3	Can be set	0x0000_004C	FLASH interrupt
RCM	4	Can be set	0x0000_0050	RCM interrupt
EINT0_1	5	Can be set	0x0000_0054	EINT line [1:0] interrupt
EINT2_3	6	Can be set	0x0000_0058	EINT line [3:2] interrupt
EINT4_15	7	Can be set	0x0000_005C	EINT line [15:4] interrupt
-	8	-	0x0000_0060	Reserved
DMA_CH1	9	Can be set	0x0000_0064	DMA channel 1 interrupt
DMA_CH2_3	10	Can be set	0x0000_0068	DMA Channel 2 and 3 interrupt
DMA_CH4_5	11	Can be set	0x0000_006C	DMA Channel 4 and 5 interrupt
ADC	12	Can be set	0x0000_0070	ADC interrupt
TMR1_BRK_UP_TRG_COM	13	Can be set	0x0000_0074	TMR1, BRK, UP, TRG and COM interrupt
TMR1_CC	14	Can be set	0x0000_0078	TMR1 capture/compareinterrupt
-	15	-	0x0000_007C	Reserved
TMR3	16	Can be set	0x0000_0080	TMR3 interrupt
TMR6	17	Can be set	0x0000_0084	TMR6 interrupt
-	18	Can be set	0x0000_0088	Reserved
TMR14	19	Can be set	0x0000_008C	TMR14 interrupt
TMR15	20	Can be set	0x0000_0090	TMR15 interrupt
TMR16	21	Can be set	0x0000_0094	TMR16 interrupt
TMR17	22	Can be set	0x0000_0098	TMR17 interrupt
I2C1	23	Can be set	0x0000_009C	I2C1 interrupt
I2C2	24	Can be set	0x0000_00A0	I2C2 interrupt
SPI1	25	Can be set	0x0000_00A4	SPI1 interrupt
SPI2	26	Can be set	0x0000_00A8	SPI2 interrupt
USART1	27	Can be set	0x0000_00AC	USART1 interrupt
USART2	28	Can be set	0x0000_00B0	USART2 interrupt
-	29	Can be set	0x0000_00B4	Reserved
-	30	Can be set	0x0000_00B8	Reserved
-	31	Can be set	0x0000_00BC	Reserved

8 External Interrupt and Event Controller (EINT)

8.1 Introduction

The interrupts/events contain internal interrupt/event and external interrupt/event. In this manual, external interrupt refers to the interrupt/event caused by I/O pin input signal, which is EINTx in interrupt vector table; other interrupts are internal interrupts/events.

The events can be divided into hardware events and software events. Hardware events are generated by external/core hardware signals, while software events are generated by instructions.

Interrupts need to go through the interrupt handler function to realize the work to be processed, while events do not need to go through interrupt handler function, and the preset work can be triggered by hardware. The external events output pulse through events such as GPIO, while the internal events trigger another TMR to work, for example, through update event of one TMR.

8.2 Functional Description

8.2.1 "External Interrupt and Event" Classification and Difference Points

"External interrupt and event" can be classified into external hardware interrupt, external hardware event, external software event and external software interrupt according to trigger source, configuration and execution process. The difference points are shown in the table below:

Table 28 "External Interrupt and Event" Classification and Difference Points

Name	Trigger source	Configuration and execution process
External hardware interrupt	External signal	(1) Set the trigger mode, allow the interrupt request, and enable corresponding peripheral interrupt line (enable in NVIC); (2) When an edge consistent with the configuration is generated on the external interrupt line, an interrupt request will be generated, and the corresponding suspend bit will be set to 1. Write 1 to the corresponding bit of the pending register and the interrupt request will be cleared.
External hardware event	External signal	(1) Set the trigger mode and enable the event line; (2) When an edge consistent with the configuration is generated on the external interrupt line, one event request pulse will be generated, and the corresponding pending bit will not be set to 1.
External software request	Software interrupt register/transmission event (SEV) instruction	(1) Enable the event line; (2) Write 1 to the software interrupt event register of the corresponding event line to generate an event request pulse, and the corresponding pending bit will not be set to 1.
External software interrupt	Software interrupt register	(1) Allow interrupt request, and enable the corresponding peripheral interrupt line (enable in NVIC); (2) Write 1 to the software interrupt event register of the corresponding event line to generate an interrupt request, the corresponding pending bit will be set to 1; write 1 to the corresponding bit of the pending register and the interrupt request will be cleared.

8.2.2 Core Wake-up

Using WFI and WFE instructions can make the core stop working. When WFI instruction is used, any interrupt can wake up the core; when WFE instruction is used, the core can be wakened up by event.

When interrupt is used for wake-up, the interrupt handler function will be triggered, and normal interrupt configuration can wake up the core. When an event is used to wake up the core, the interrupt handler function will not be triggered, which will reduce the wake-up time, and the configuration method is:

（1） It can trigger an internal interrupt (internal hardware event) but cannot trigger the interrupt handler function for wake-up
- It can enable an internal interrupt in the peripheral, but cannot enable the corresponding interrupt in NVIC to avoid triggering the interrupt handler function
- Enable SEVONPEND bit in the system controller of the core, and execute WFE instruction to make the core enter sleep mode
- Generate an interrupt to wake up the core; when the core recovers from WFE, it is required to clear the pending bit of corresponding peripheral interrupt and the pending bit of peripheral NVIC interrupt channel (clear the pending register in the NVIC interrupt)

（2） Wake up through EINT line events (external hardware event)
- Configure EINT line as the event mode
- Execute WFE instruction to make the core enter the sleep mode
- Generate an interrupt to wake up the core; when the CPU recovers from WFE, since the pending bit of corresponding event line is not set, it is unnecessary to clear the interrupt pending bit of corresponding peripheral or the NVIC interrupt channel pending bit

8.2.3 External Interrupt and Event Line Mapping

Table 29 External Interrupt and Event Line Mapping

External Interrupt and Event Channel Name	External Interrupt and Event Line No.
PA0/PB0/PC0/PF0	EINT 0
PA1/PB1/PC1/PF1	EINT 1
PA2/PB2/PC2/PD2	EINT 2
PA3/PB3/PC3	EINT 3
PA4/PB4/PC4/PF4	EINT 4
…	…
PA7/PB7/PC7/PF7	EINT 7
PA8/PB8/PC8	EINT 8
…	…
PA15/PB15/PC15	EINT 15
Reserved	EINT 16
RTC alarm event	EINT 17
Reserved	EINT 18
RTC Clock intrusion and timestamp event	EINT 19
RTC wake-up event	EINT 20
Reserved	EINT 21~31

Note: Vacant GPIO channel, because there is no corresponding GPIO pin, its corresponding register bit is reserved.

8.3 Register Address Mapping

Table 30 External Interrupt/Event Controller Register Mapping

Register name	Description	Offset address
EINT_IMASK	Interrupt mask register	0x00
EINT_EMASK	Event mask register	0x04
EINT_RTEN	Enable the rising edge trigger selection register	0x08
EINT_FTEN	Enable the falling edge trigger selection register	0x0C
EINT_SWINTE	Software interrupt event register	0x10
EINT_IPEND	Interrupt pending register	0x14

8.4 Register Functional Description

8.4.1 Interrupt mask register (EINT_IMASK)

Offset address: 0x00

Reset value: 0x7F84 0000

Field	Name	R/W	Description
31:0	IMASKx	R/W	Interrupt request on mask line x (Interrupt Request Mask on Line x) 0: Mask 1: Open

8.4.2 Event mask register (EINT_EMASK)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	EMASKx	R/W	Event request on mask line x (Event Request Mask on Line x) 0: Mask 1: Open

8.4.3 Enable the rising edge trigger selection register (EINT_RTEN)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	RTENx	R/W	Enable the rising trigger event and interrupt on Line x (Rising Trigger Event Enable and Interrupt of Line x) 0: Disable 1: Enable
16	Reserved		

Field	Name	R/W	Description
17	RTENx	R/W	Enable the rising trigger event and interrupt on Line x (Rising Trigger Event Enable and Interrupt of Line x) 0: Disable 1: Enable
18	Reserved		
20:19	RTEN31	R/W	Enable the rising trigger event and interrupt on Line 31 (Rising Trigger Event Enable and Interrupt of Line 31) 0: Disable 1: Enable
31:21	Reserved		

Note: Since the external wake-up lines are edge triggered, there should be no burr signal on these lines; when writing EINT_RTEN register, if the rising edge signal is on the external interrupt line, it will not be recognized and the set pending bit will not be set; in the same interrupt line, the rising edge trigger and falling edge trigger can be set at the same time.

8.4.4 Enable the falling edge trigger selection register (EINT_FTEN)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	FTENx	R/W	Enable the falling trigger event and interrupt on Line x (Falling Trigger Event Enable and Interrupt of Line x) 0: Disable 1: Enable
16	Reserved		
17	FTENx	R/W	Enable the falling trigger event and interrupt on Line x (Falling Trigger Event Enable and Interrupt of Line x) 0: Disable 1: Enable
18	Reserved		
20:19	FTEN31	R/W	Enable the falling trigger event and interrupt on Line 31 (Falling Trigger Event Enable and Interrupt of Line 31) 0: Disable 1: Enable
31:21	Reserved		

Note: Since the external wake-up lines are edge triggered, there should be no burr signal on these lines; when writing EINT_FTEN register, if the rising edge signal is on the external interrupt line, it will not be recognized and the set pending bit will not be set; in the same interrupt line, the rising edge trigger and falling edge trigger can be set at the same time.

8.4.5 Software interrupt event register (EINT_SWINTE)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	SWINTEx	R/W	Software interrupt on Line x (Software Interrupt Event on Line x) This bit can be set to 1 by software, and be cleared by writing 1 to the corresponding bit of EINT_IPEND.

Field	Name	R/W	Description
			When this bit is 0, the pending bit of EINT_IPEND can be set by writing 1. If EINT_IMASK (EINT_EMASK) is set to open the interrupt (event) request, an interrupt (event) will be generated. 0: No effect 1: Software generates an interrupt (event)
16	Reserved		
17	SWINTEx	R/W	Software interrupt on Line x (Software Interrupt Event on Line x) This bit can be set to 1 by software, and be cleared by writing 1 to the corresponding bit of EINT_IPEND. When this bit is 0, the pending bit of EINT_IPEND can be set by writing 1. If EINT_IMASK (EINT_EMASK) is set to open the interrupt (event) request, an interrupt (event) will be generated. 0: No effect 1: Software generates an interrupt (event)
18	Reserved		
20:19	SWINTE31	R/W	Software interrupt on Line 31 (Software Interrupt Event on Line 31) This bit can be set to 1 by software, and be cleared by writing 1 to the corresponding bit of EINT_IPEND. When this bit is 0, the pending bit of EINT_IPEND can be set by writing 1. If EINT_IMASK (EINT_EMASK) is set to open the interrupt (event) request, an interrupt (event) will be generated. 0: No effect 1: Software generates an interrupt (event)
31:21	Reserved		

8.4.6 Pending register (EINT_IPEND)

Offset address: 0x14

Reset value: 0xXXXX XXXX

Field	Name	R/W	Description
15:0	IPENDx	RC_W1	Interrupt Pending Occur of Line x Flag Whether the selected trigger request occurs 0: None 1: Occurred When a trigger request on the corresponding edge of EINT occurs on an external interrupt line, it will be set to 1 by hardware; it can be cleared by changing the polarity of the edge detection or by writing 1 to this bit.
16	Reserved		
17	IPENDx	RC_W1	Interrupt Pending Occur of Line x Flag Whether the selected trigger request occurs 0: None 1: Occurred When a trigger request on the corresponding edge of EINT occurs on an external interrupt line, it will be set to 1 by hardware; it can be cleared by changing the polarity of the edge detection or by writing 1 to this bit.
18	Reserved		

Field	Name	R/W	Description
20:19	IPEND31	RC_W1	Interrupt Pending Occur of Line 31 Flag Whether the selected trigger request occurs 0: None 1: Occurred When a trigger request on the corresponding edge of EINT occurs on an external interrupt line, it will be set to 1 by hardware; it can be cleared by changing the polarity of the edge detection or by writing 1 to this bit.
31:21	Reserved		

9 Direct Memory Access (DMA)

9.1 Full Name and Abbreviation Description of Terms

Table 31 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Global	G
Transfer	T
Half	H
Complete	C
Error	E
Channel	CH
Circular	CIR
Peripheral	PER
Increment	I
Memory	M
Priority	PRI
Number	N
Address	ADDR

9.2 Introduction

DMA (Direct Memory Access) can realize direct data transmission between peripheral devices and memory or between memory and memory without CPU intervention, thus saving CPU resources for other operations.

DMA has a controller, which has five channels. Each channel can manage multiple DMA requests, but each channel can only start one DMA request at the same time. Each channel can set priority, and the arbiter can coordinate the priority of corresponding DMA requests of each DMA channel according to the priority of the channels.

9.3 Main Characteristics

（1） DMA has five channels

（2） There are three data transmission modes: peripheral to memory, memory to peripheral, memory to memory

（3） Each channel has a special hardware DMA request for connection

（4） Support software priority and hardware priority when multiple requests occur at the same time

（5） Each channel has three event flags and independent interrupts

（6） Support circular transmission mode

（7） The number of data transmission is programmable, up to 65535

9.4 Functional Description

9.4.1 DMA Request

If the peripheral or memory needs to use DMA to transmit data, it is required to first send DMA request and wait for DMA approval before data transmission.

DMA has five channels. Each channel is connected with different peripherals, and each channel has three event flags (DMA half transmission, DMA transmission completion and DMA transmission error). The logic of the three event flags may become a separate interrupt request, and they all support software triggering.

When multiple peripherals request the same channel, it is required to configure the corresponding register to turn on or off the request of each peripheral, so as to ensure that only one peripheral request can be turned on in a channel.

Table 32 DMA Request Mapping Table 1

Peripheral	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
TMR1	-	TMR1_CH1	TMR1_CH2	TMR1_CH4 TMR1_TRIG TMR1_COM	TMR1_CH3 TMR1_UP
TMR3	-	TMR3_CH3	TMR3_CH4 TMR3_UP	TMR3_CH1 TMR3_TRIG	-
TMR6	-	-	TMR6_UP	-	-
TMR15	-	-	-	-	TMR15_CH1 TMR15_UP TMR15_TRIG TMR15_COM
TMR16	-	-	TMR16_CH1(1) TMR16_UP(1)	TMR16_CH1(2) TMR16_UP(2)	-
TMR17	TMR17_CH1(1) TMR17_UP(1)	TMR17_CH1(2) TMR17_UP(2)	-	-	-
ADC	ADC(1)	ADC(2)	-	-	-
SPI	-	SPI1_RX	SPI1_TX	SPI2_RX	SPI2_TX

Peripheral	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
USART	-	USART1_TX(1)	USART1_RX(1)	USART1_TX(2) USART2_TX	USART1_RX(2) USART2_RX
I2C	-	I2C1_TX	I2C1_RX	I2C2_TX	I2C2_RX

Note: (1) This DMA request is mapped to the DAM channel only when the corresponding remapping bit of SYSCFG_CFGR1 register is cleared.

(2) This DMA request is mapped to the DAM channel only when the corresponding remapping bit of SYSCFG_CFGR1 register is set.

9.4.2 DMA Channel

9.4.2.1 Transmission data are programmable

The data transmitted by DMA are programmable, up to 65535, and the transmission data bit width of peripherals and memory can be set by configuring PERSIZE bit and MSIZE bit of DMA_CHCFGx register.

9.4.2.2 Transmission width and alignment method are programmable

Programmable data transmission width DMA transmission operations:

Figure 8 Transmission Width with Source of 8bits and Target of 8bits

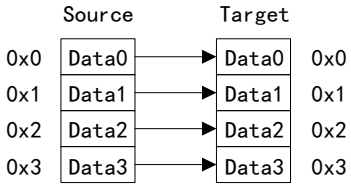


Figure 9 Transmission Width with Source of 8bits and Target of 16bits

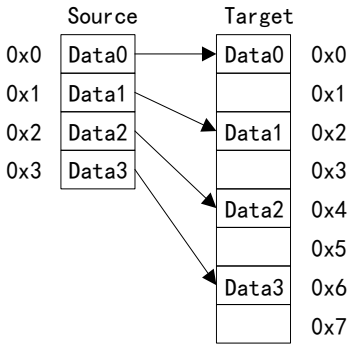


Figure 10 Transmission Width with Source of 8bits and Target of 32bits

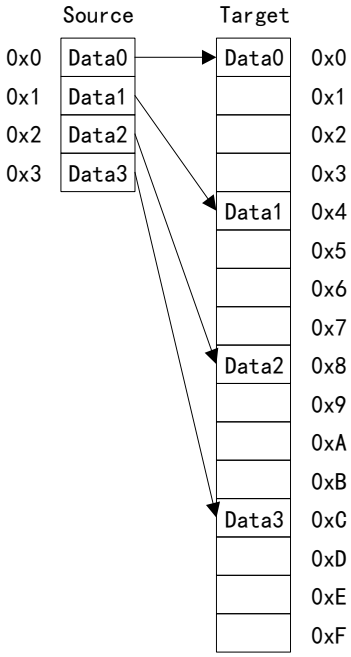


Figure 11 Transmission Width with Source of 32bits and Target of 8bits

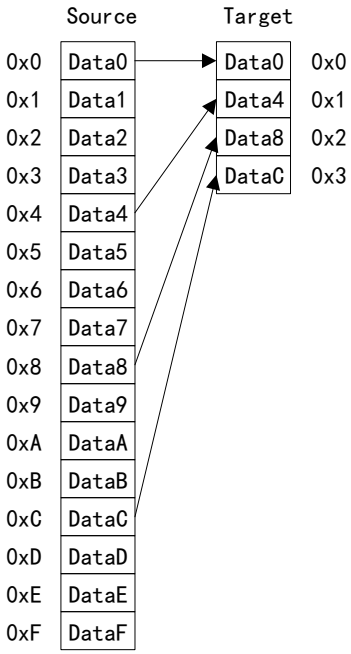


Figure 12 Transmission Width with Source of 16bits and Target of 16bits

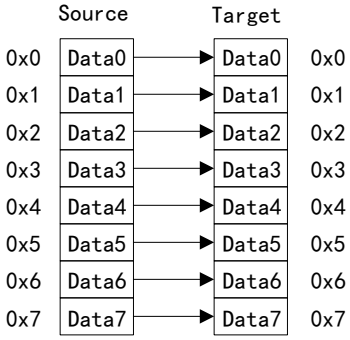


Figure 13 Transmission Width with Source of 16bits and Target of 32bits

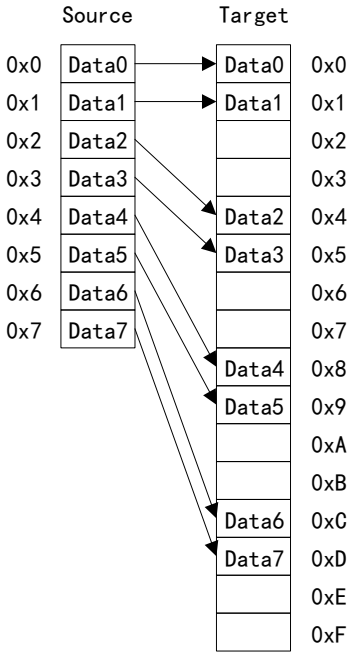
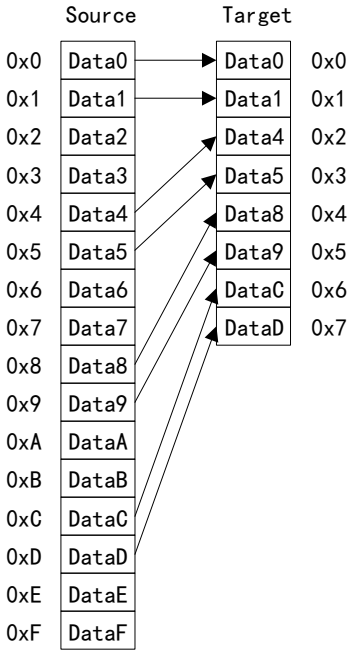


Figure 14 Transmission Width with Source of 32bits and Target of 16bits



9.4.2.3 Address setting

The transmission address supports two modes: fixed mode and pointer increment mode.

Transmission address pointer increment mode

The automatic pointer increment of peripheral and memory is completed through the PERIMODE bit and MIMODE bit of configuration register DMA_CHCFGx. The next address to be transmitted is the one by adding the increment to the previous address. The increment depends on the selected data width.

9.4.2.4 Transmission mode

There are two channel configuration modes: non-circular mode and circular mode.

Non-circular mode

When the data transmission is finished, the DMA operation will not be performed any more, and the new DMA transmission will be started. When the DMA channel is not working, the register DMA_CHNDATAx will rewrite the transmission value.

Circular mode

After data transmission, the content of the register DMA_CHNDATAx will be automatically reloaded to the previously configured value, and the peripheral address register DMA_CHPADDRx and the memory address register DMA_CHMADDRx will also be reloaded as the initial base address.

The configuration method is as follows:

- Set the CIRMODE bit of the configuration register DMA_CHCFGx to 1 to turn on the circular mode
- This mode is used to process continuous peripheral requests. When the number of data transmission becomes 0, it will automatically return to the initial value and continue DMA operation until the CIRMODE bit is cleared and the system exits the circular mode

9.4.2.5 DMA request priority setting

Arbitrator

When multiple DMA channel requests occur, an arbiter is needed to manage the response sequence. Management is divided into two stages: the first stage is software stage, which is divided into the highest, high, medium and low priority; the second stage is hardware stage, and under the condition of the same software priority, the lower the channel number is, the higher the priority is.

9.4.2.6 Transmission direction

Support three directions: from memory to memory, from memory to peripheral, and from peripheral to memory.

If the write operation (target address) is performed on the memory, the memory includes external RAM supported by internal SRAM (such as external SRAM); if the read operation (source address) is performed on the memory, the address includes internal FLASH and internal SRAM.

Examples of "from memory to memory" configuration are as follows:

- The M2MMODE bit of the configuration register DMA_CHCFGx is set to put the memory to the memory mode
- The DMA operation in this mode is performed under the condition of no peripheral request. The CHEN bit of the configuration register DMA_CHCFGx is set to 1, and after the channel is opened, the data transmission will start and when the transmission quantity register DMA_CHNDATAx becomes 0, the transmission is over

9.4.3 Interrupt

Each DMA channel has three types of interrupt events, which are half transmission (HT), transmission completion (TC) and transmission error (TE).

（1） The interrupt event flag bit for half transmission is HTFLG, and the interrupt enable control bit is HTINTEN

（2） The interrupt event flag bit for transmission completion is TCFLG, and the interrupt enable control bit is TCINTEN

（3） The interrupt event flag bit for transmission error is TERRFLG, and the interrupt enable control bit is TERRINTEN

9.5 Register Address Mapping

Table 33 DMA Register Address Mapping

Register name	Description	Offset address
DMA_INTSTS	DMA interrupt state register	0x00
DMA_INTFCLR	DMA interrupt flag clear register	0x04
DMA_CHCFGx	DMA Channel x configuration register	0x08+ 20 x
DMA_CHNDATAx	DMA Channel x transmission quantity register	0x0C+ 20 x
DMA_CHPADDRx	DMA Channel x peripheral address register	0x10+ 20 x
DMA_CHMADDRx	DMA Channel x memory address register	0x14 + 20 x
DMA_CHSEL	DMA channel selection register	0xA8

9.6 Register Functional Description

9.6.1 DMA interrupt state register (DMA_INTSTS)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
16，12，8，4，0	GINTFLGx	R	ChannelxGlobal Interrupt Occur Flag (x=1…5) Indicate whether TC, HT or TE interrupt is generated on the channel; these bits are set to 1 by hardware; write 1 and clear on the corresponding bit of DMA_INTFCLR. 0: Not generate 1: Generate
17，13，9，5，1	TCFLGx	R	ChannelxAll Transfer Complete Flag (x=1…5) Indicate whether the transmission completion interrupt (TC) is generated on the channel; these bits are set to 1 by hardware; write 1 and clear on the corresponding bit of DMA_INTFCLR. 0: Not completed 1: Completed
18，14，10，6，2	HTFLGx	R	ChannelxHalf Transfer Complete Flag (x=1…5) Indicate whether the half transmission interrupt (HT) is generated on the channel; these bits are set to 1 by hardware; write 1 and clear on the corresponding bit of DMA_INTFCLR. 0: Not generate 1: Generate
19，15，11，7，3	TERRFLGx	R	ChannelxTransfer Error Occur Flag (x=1…5) Indicate whether the transmission error interrupt (TE) is generated on the channel; these bits are set to 1 by hardware; write 1 and clear on the corresponding bit of DMA_INTFCLR. 0: Not generate 1: Generate
31:20	Reserved		

9.6.2 DMA interrupt flag clear register (DMA_INTFCLR)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
16，12，8，4，0	GINTCLRx	W	ChannelxGlobal Interrupt Occur Flag Clear (x=1…5) Clear the corresponding GINTFLG, TCFLG, HTFLG and TERRFLG flags in the interrupt state register. 0: Invalid 1: Clear the GINTFLG flag
17，13，9，5，1	TCCLRx	W	ChannelxTransfer Complete Clear (x=1…5) Clear the corresponding TCFLG flag in interrupt state register. 0: Invalid 1: Clear the TCFLG flag

Field	Name	R/W	Description
18，14，10，6，2	HTCLRx	W	ChannelxHalf Transfer Complete Clear (x=1…5) Clear the corresponding HTFLG flag in interrupt state register. 0: Invalid 1: Clear the HTFLG flag
19，15，11，7，3	TERRCLRx	W	ChannelxTransfer Error Occur Clear (x=1…5) Clear the corresponding TERRFLG flag in interrupt state register. 0: Invalid 1: Clear the TERRFLG flag
31:20	Reserved		

9.6.3 DMA Channel x configuration register (DMA_CHCFGx) (x=1…5)

Offset address: 0x08+20 x (channel number-1)

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	CHEN	R/W	DMA Channel Enable 0: Disable 1: Enable
1	TCINTEN	R/W	All Transfer Complete Interrupt Enable 0: Disable 1: Enable
2	HTINTEN	R/W	Half Transfer Complete Interrupt Enable 0: Disable 1: Enable
3	TERRINTEN	R/W	Transfer Error Occur Interrupt Enable 0: Disable 1: Enable
4	DIRCFG	R/W	Data Transfer Direction Configure 0: Read from peripheral to memory 1: Read from memory to peripheral
5	CIRMODE	R/W	Circular Mode Enable 0: Disable 1: Enabl
6	PERIMODE	R/W	Peripheral Address Increment Mode Enable 0: Disable 1: Enable
7	MIMODE	R/W	Memory Address Increment Mode Enable 0: Disable 1: Enable
9:8	PERSIZE	R/W	Peripheral Data Size Configure 00: 8 bits 01: 16 bits 10: 32 bits 11: Reserved
11:10	MSIZE	R/W	Memory Data Size Configure 00: 8 bits 01: 16 bits 10: 32 bits 11: Reserved

Field	Name	R/W	Description
13:12	CHPL	R/W	Channel Priority Level Configure 00: Low 01: Medium 10: High 11: Highest
14	M2MMODE	R/W	Memory to Memory Mode Enable 0: Disable 1: Enable
31:15	Reserved		

9.6.4 DMA Channel x transmission quantity register (DMA_CHNDATAx) (x=1…5)

Offset address: 0x0C+20 x (channel number-1)

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	NDATAT	R/W	Number of Data to Transfer Setup This register indicates the number of bytes to be transmitted. The number of data transmission ranges from 0 to 65535. This register can only be written when the channel is not working; once the channel is enabled, the register will be read-only, indicating the number of remaining bytes to be transmitted. The register will decrease after each DMA is transmitted; when the data transmission is completed, the register will change to 0, or when the channel is configured to auto reload mode, it will be automatically reloaded to the previously configured value; if the register is 0, data transmission will not occur regardless of whether the channel is turned on or not.
31:16	Reserved		

9.6.5 DMA Channel x peripheral address register (DMA_CHPADDRx) (x=1…5)

Offset address: 0x10+20 x (channel number-1)

Reset value: 0x0000 0000

This register cannot be written when the channel is turned on (CHEN=1 for DMA_CHCFGx).

Field	Name	R/W	Description
31:0	PERADDR	R/W	Peripheral Basic Address Setup When PERSIZE= '01' (16 bits) and PERADDR[0] bit is not used, it will be aligned with 16-bit address automatically during transmission. When PERSIZE= '10' (32 bits) and PERADDR[1:0] bit is not used, it will be aligned with 32-bit address automatically during transmission.

9.6.6 DMA Channel x memory address register (DMA_CHMADDRx) (x=1…5)

Offset address: 0x14+20 x (channel number-1)

Reset value: 0x0000 0000; when the channel is turned on (CHEN=1 for DMA_CHCFGx), this register cannot be written.

Field	Name	R/W	Description
31:0	MEMADDR	R/W	Memory Basic Address Setup

Field	Name	R/W	Description
			When MSIZE= '01' (16 bits) and MEMADDR[0] bit is not used, it will be aligned with 16-bit address automatically during transmission. When MSIZE= '10' (32 bits) and MEMADDR[1:0] bit is not used, it will be aligned with 32-bit address automatically during transmission.

10 Debug MCU (DBGMCU)

10.1 Full Name and Abbreviation Description of Terms

Table 34 Full Name and Abbreviation Description of DBGMCU Terms

Full name in English	English abbreviation
Frame Clock	FCLK
Data Watchpoint Trigger	DWT
Break Point Unit	BPU

10.2 Introduction

APM32F030 series uses Arm® Cortex®-M0+ core, and Arm® Cortex® -M0+ core includes hardware debug module and supports complex debug operation. During debugging, the module can make the running core stop at breakpoint, and achieve the effect of querying the internal state of the core and the external state of the system, and after the query is completed, the core and peripheral operation can be restored to continue to execute the program.

Supported debugging interface: serial interface

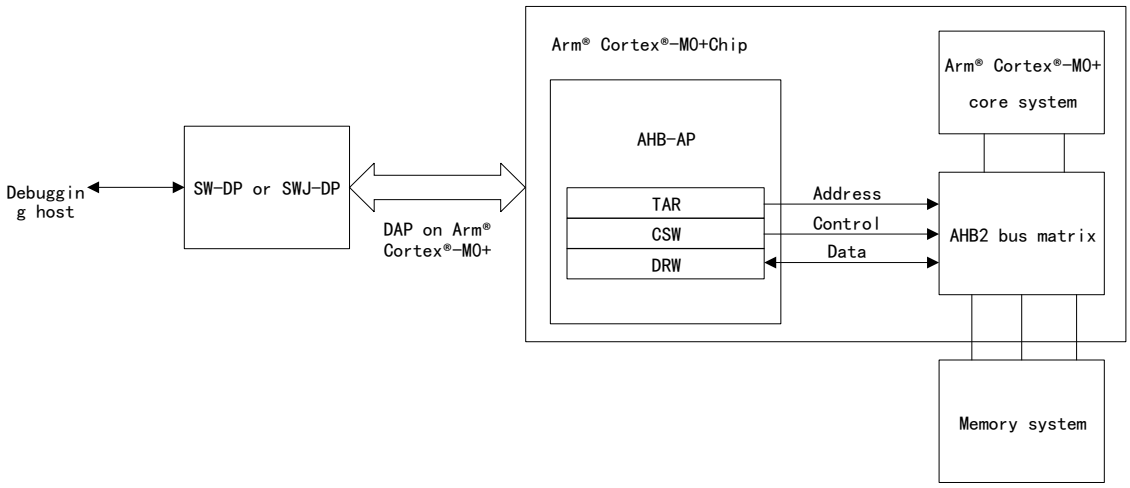
Note: The hardware debug interface included in Arm® Cortex® -M0 core is subset of Arm CoreSight development tool set. Please refer to *Cortex®-M0+ (Version r1p1) Technical Reference Manual (TRM)* and *CoreSight Development Tool Set (Version r1p0) TRM* for more information about debug function of Arm® Cortex®-M0+ core.

10.3 Main Characteristics

（1） Flexible debug pin assignment

（2） MCU de1wer mode, control peripheral clock, etc.

Figure 15 APM32F0xx Level and Arm® Cortex®-M0+ Level Debugging Block Diagram



10.4 Functional Description

（1） Realize the on-line programming and debugging of the chip

（2） Using KEIL/IAR and other software to achieve on-line debugging, downloading and programming

（3） Flexible implementation of production of bus-line programmer

10.5 Register Address Mapping

Table 35 DBGMCU Register Address Mapping

Register name	Description	Offset address
DBGMCU_IDCODE	Debug MCU device ID register	0x4001 5800
DBGMCU_CFG	Debug MCU configuration register	0x4001 5804
DBGMCU_APB1F	Debug MCU APB1 freeze register	0x4001 5808
DBGMCU_APB2F	Debug MCU APB2 freeze register	0x4001 580C

10.6 Register Functional Description

10.6.1 Debug MCU device ID register (DBGMCU_IDCODE)

Address: 0x4001 5800

Only support 32-bit access

Reset value: 0xXXXX XXXX

Field	Name	R/W	Description
11:0	EQR	R	Equipment Recognition APM32E030 microcontroller series:0x440 The debugger/programming tool identifies chips by QR (11:0).
15:12	Reserved		
31:16	WVR	R	Wafer Version Recognition APM32E030 microcontroller series: Products Version A: 0x0010

10.6.2 Debug MCU configuration register (DBGMCU_CFG)

This register allows MCU to be configured during debugging and supports low-power mode.

It is reset asynchronously by POR (not reset by system), and it can be written by debugger through system reset.

If the debugging host does not support these characteristics, the user software can write to these registers.

Only support 32-bit access

Address: 0x4001 5804

Reset value: 0x0000 (unaffected by system reset)

Field	Name	R/W	Description
0	Reserved		
1	STOP_CLK_STS	R/W	Debug Stop Mode Configure 0: In the stop mode when both FCLK and HCLK are turned off, all clocks will be disabled by clock controller. When exiting the stop mode, the clock configuration is the same as that after reset (the clock is provided by the 8MHz internal RC oscillator HSICLK), so the software needs to reconfigure the clock controller to start PLL, crystal oscillator, etc.

Field	Name	R/W	Description
			1: In the stop mode when both FCLK and HCLK are turned on, both FCLK and HCLK are provided by internal RC oscillator. The internal RC oscillator remains or is active in the stop mode. When it exits the stop mode, the software must reconfigure the clock controller to enable PLL, crystal oscillator, etc.
2	STANDBY_CLK_STS	R/W	Debug Standby Mode 0: When both FCLK and HCLK are turned off, the digital part is not powered on. From the software level, it indicates that when the MCU just exits from the standby mode, others exit the debug mode, which is the same as reset 1: When both FCLK and HCLK are turned on, the digital part is powered on, and the internal RC oscillator provides FCLK and HCLK clocks. Besides, the MCU exits the standby mode through system reset, which is the same as reset.
31:3	Reserved		

10.6.3 Debug MCU APB1 freeze register (DBGMCU_APB1F)

This register is used to configure MCU during debugging.

Involve some APB peripherals:

- Freeze the timer counter
- Freeze I2C SMBus timeout
- Freeze supporting system window regulators and independent watchdog counters

This register is reset asynchronously by POR (instead of system reset) and can be written by the debugger through system reset.
Only support 32-bit access
Address: 0x4001 5808
Reset value: 0x0000 (unaffected by system reset)

Field	Name	R/W	Description
0	Reserved		
1	TMR3_STS	R/W	Configure TMR3 Work Status When Core is in Halted Whether TMR3 counter continues to work when the core stops work 0: Continue to work 1: Stop working
3:2	Reserved		
4	TMR6_STS	R/W	Configure TMR6 Work Status When Core is in Halted Whether TMR6 counter continues to work when the core stops work 0: Continue to work 1: Stop working
7:5	Reserved		
8	TMR14_STS	R/W	Configure TMR14 Work Status When Core is in Halted Whether TMR14 counter continues to work when the core stops work 0: Continue to work 1: Stop working
9	Reserved		

Field	Name	R/W	Description
10	RTC_STS	R/W	Configure RTC Work Status When Core Is in Halted Whether RTC counter continues to work when the core stops work 0: Continue to work 1: Stop working
11	WWDT_STS	R/W	Configure Window Watchdog Work Status When Core Is in Halted Whether WWDT continues to work when the core is halted 0: Continue to work 1: Stop working
12	IWDT_STS	R/W	Configure Independent Watchdog Work Status When Core Is in Halted Whether IWDT continues to work when the core is halted 0: Continue to work 1: Stop working
20:13	Reserved		
21	I2C1_SMBUS_TIMEOUT_STS	R/W	Configure I2C1_SMBUS_TIMEOUT Work Status When Core Is in Halted 0: Work normally 1: Freeze the timeout mode of SMBUS
31:22	Reserved		

10.6.4 Debug MCU APB2 freeze register (DBGMCU_APB2F)

This register is used to configure MCU during debugging.

Involve some APB peripherals:

- Freeze the timer counter

This register is reset asynchronously by POR (instead of system reset) and can be written by the debugger through system reset.

Only support 32-bit access

Address: 0x4001 580C

Reset value: 0x0000 (unaffected by system reset)

Field	Name	R/W	Description
10:0	Reserved		
11	TMR1_STS	R/W	Configure TMR1 Work Status When Core is in Halted Whether TMR1 counter continues to work when the core stops work 0: Continue to work 1: Stop working
15:12	Reserved		
16	TMR15_STS	R/W	Configure TMR15 Work Status When Core is in Halted Whether TMR15 counter continues to work when the core stops work 0: Continue to work 1: Stop working
17	TMR16_STS	R/W	Configure TMR16 Work Status When Core is in Halted Whether TMR16 counter continues to work when the core stops work 0: Continue to work 1: Stop working
18	TMR17_STS	R/W	Configure TMR17 Work Status When Core is in Halted Whether TMR17 counter continues to work when the core stops work 0: Continue to work 1: Stop working

Field	Name	R/W	Description
31:19	Reserved		

11 General-purpose Input/Output Pin (GPIO)

11.1 Full Name and Abbreviation Description of Terms

Table 36 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
P-channel Metal Oxide Semiconductor	P-MOS
N-channel Metal Oxide Semiconductor	N-MOS

11.2 Main Characteristics

The GPIO port can be configured with the following functions via the 32-bit configuration register (GPIOx_MODE/GPIOx_OMODE/GPIOx_OSSEL/GPIOx_PUPD) and two 32-bit data registers (GPIOx_IDATA/GPIOx_ODATA) :

（1） Input mode
- Floating input
- Pull-up input
- Pull-down input

（2） Output mode
- Push-pull output
- Open-drain output
- Configurable maximum output rate

（3） Multiplexing mode
- Push-pull multiplexing function
- Open-drain multiplexing function

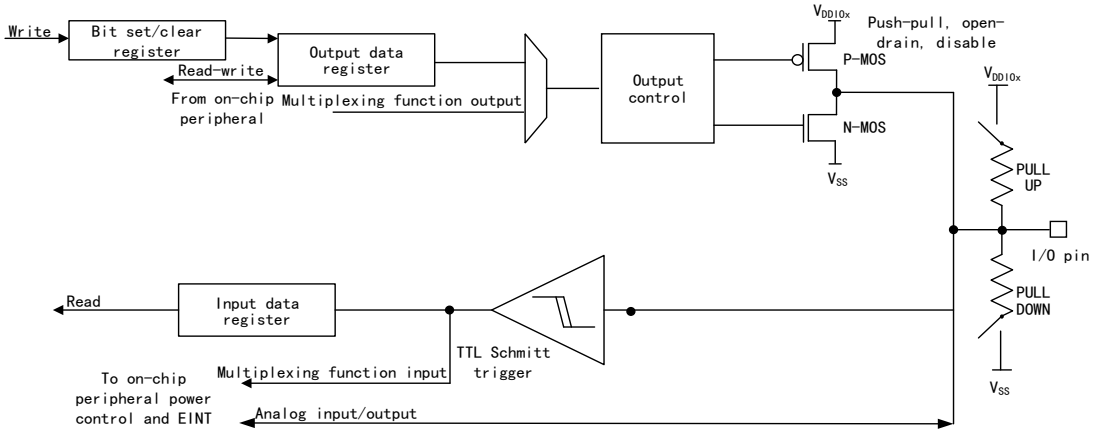
（4） Analog mode

（5） GPIO can be used as external interrupt/wake-up line

（6） Support locking I/O configuration function

11.3 Structure Block Diagram

Figure 16 GPIO Structure Block Diagram



11.4 Functional Description

Each pin of GPIO can be configured as pull-up, pull-down, floating and analog input, or push-pull/open-drain output input mode and multiplexing function through software. All GPIO interfaces have external interrupt capability.

11.4.1 IO Status during Reset and just after Reset

During and just after GPIO reset, if the multiplexing function is not turned on, the I/O port will be configured as floating input mode. After reset, the debug pin is placed in input pull-up or pull-down mode, which is configured as follows:

- PA13: SWDIO in pull- up mode
- PA14: SWCLK in pull- down mode

11.4.2 Input Mode

In the input mode, it can be set as pull-up, pull-down, floating and analog input.

When GPIO is configured as input mode, all GPIO pins have internal weak pull-up and weak pull-down resistors, which can be activated or disconnected.

Pull-up, pull-down, and floating modes

In (pull-up, pull-down, floating) input mode

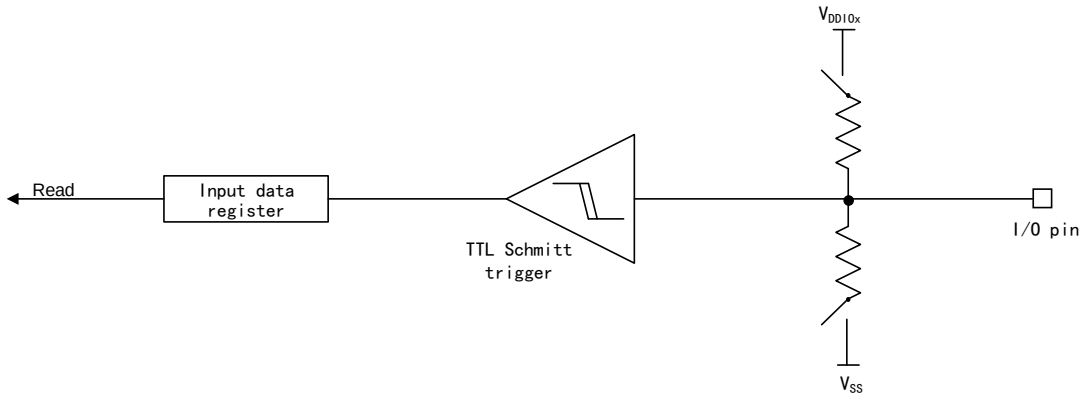
- Schmitt trigger is opened,
- Disable output buffer
- By configuring the pull-up/pull-down register GPIOx_PUPD, select whether to use pull-up/pull-down resistors
- The input data register GPIOx_IDATA captures the data on I/O pin in each AHB clock cycle.
- Read I/O state through the input data register GPIOx_IDATA

The initial level state of the floating input mode is uncertain and is easy to be disturbed by the outside; when connecting the equipment, it is determined by the external input level (except for the very high impedance).

The initial level state of pull-up/pull-down input mode is high level if pull-up, and

low level if pull-down; when connecting the equipment, it is determined by the external input level and load impedance.

Figure 17 I/O Structure in Input Mode



11.4.3 Output Mode

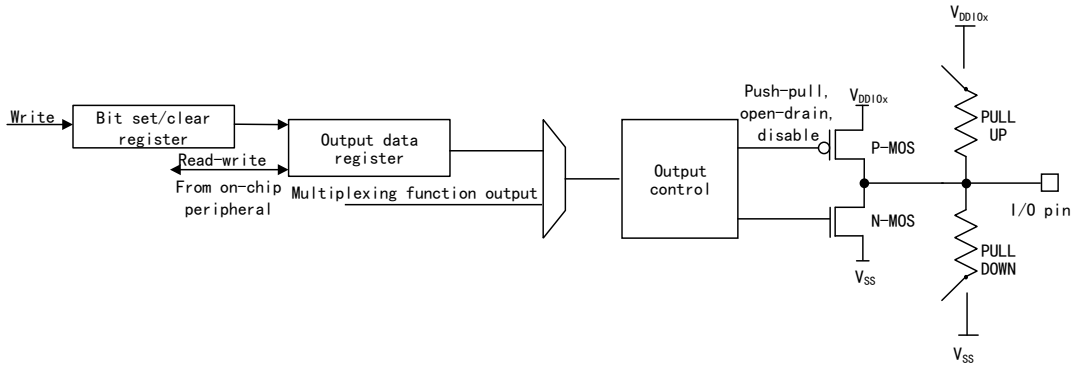
In the output mode, it can be set as push-pull output and open-drain output.

When GPIO is configured as the output pin, the output speed of the port can be configured and the output drive mode (push-pull / open-drain) can be selected.

In output mode:

- Schmitt trigger is opened,
- Activate output buffer
- By configuring the pull-up/pull-down register GPIOx_PUPD, select whether to use pull-up/pull-down resistors
- Push-pull mode:
  - Double MOS transistor works by turns and the output data register can control the high and low level of I/O output
  - Read the finally written value through the output data register GPIOx_ODATA
- Open-drain mode:
  - Only N-MOS works, and the output data register can control I/O output high resistance state or low level
  - The input data register GPIOx_IDATA captures the data on I/O pin in each AHB clock cycle
  - Read the actual I/O state through the input data register GPIOx_IDATA

Figure 18 I/O Structure in Output Mode



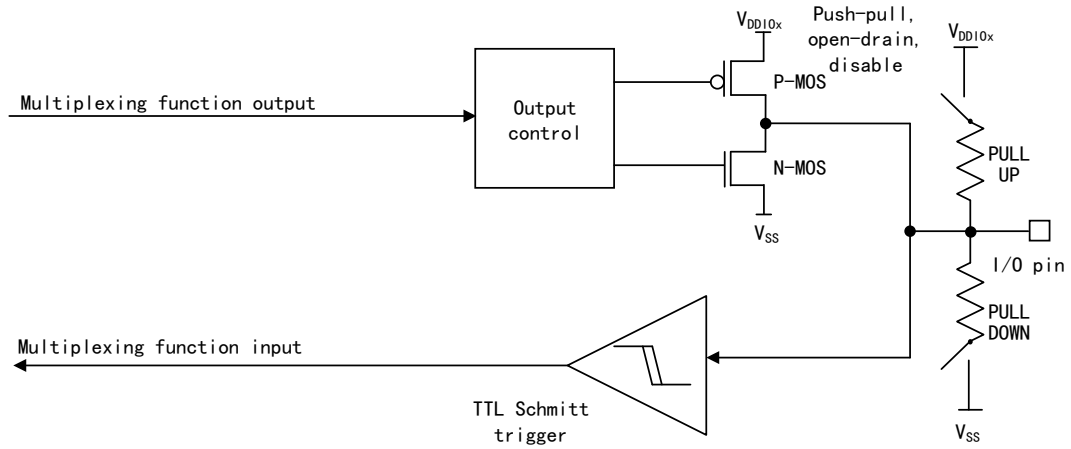
11.4.4 Multiplexing Mode

In multiplexing mode, it can be set as push-pull multiplexing and open-drain multiplexing

In push-pull/open-drain multiplexed mode:

- Open the output buffer
- Output buffer is driven by peripheral
- Activate schmitt trigger input
- By configuring the pull-up/pull-down register GPIOx_PUPD, select whether to use pull-up/pull-down resistors
- The data on the I/O pin is sampled in each AHB clock cycle and stored in the port input state register
- Read the actual I/O state through the input data register GPIOx_IDATA

Figure 19 I/O Structure in Multiplexing Mode

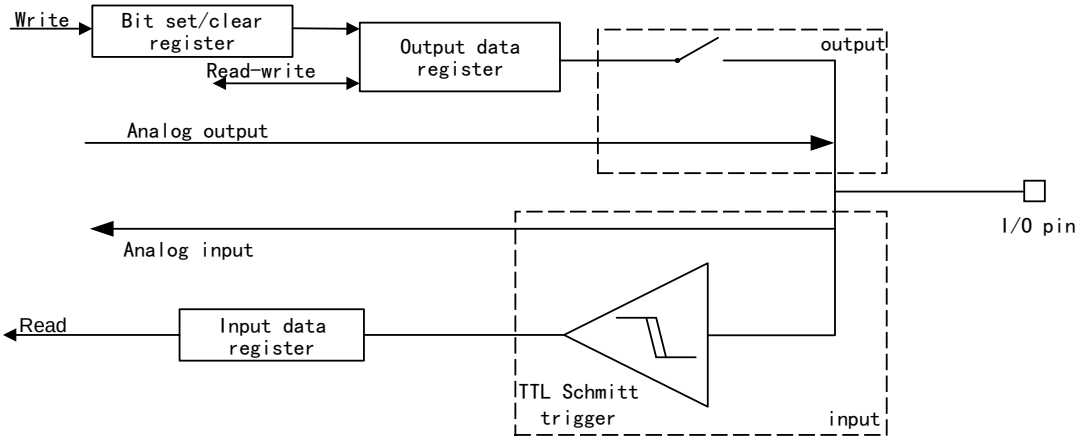


11.4.5 Analog Mode

In analog function mode:

- Disable output buffer
- The input of Schmitt trigger is disabled, and the output value of Schmitt trigger is forced to be 0
- Weak pull-up and pull-down resistors are disabled
- Read the value of the input state register to be 0

Figure 20 Analog Function I/O Structure



11.4.6 External Interrupt/Wake-up Line

All GPIO ports have external interrupt function. If you want to use external interrupt line, the port must be configured as input mode.

11.4.7 I/O Data Bit Processing

GPIO port set/reset register (GPIOx_BSC) allows set/reset operation for each bit of the output data register (GPIOx_ODATA). The valid data width of the set/reset register is double the valid data width of GPIOx_ODATA.

Writing 0 to any bit in GPIOx_BSC will not affect the value of the GPIOx_ODATA register. If BS and BC bits of GPIOx_BSC are set to 1 at the same time, BS bit has the priority. GPIOx_ BSC register can change the corresponding bit of the GPIOx_ODATA register, the BS set of GPIOx_BSC corresponds to the GPIOx_ODATA position 1, and the BC set of GPIOx_BSC corresponds to the GPIOx_ODATA bit cleared to zero.

When the access mechanism is set or reset by GPIOx_ODATA through GOIOx_BSC register, it is not necessary to turn off the interrupt by software to access GPIOx_ODATA.

11.4.8 Multiplexing Function and Remapping

Multiplexer

The multiplexer is used to connect the I/O port line of the device to the embedded peripheral module, and it can only be one-to-one at the same time.

Each I/O pin is equipped with a multiplexer. The multiplexer multiplexing function input up to 16, but in APM32E030 actually use up to 7 (AF0~AF6),, which is configured by GPIOx_ALFL and GPIOx_ALFH registers. When I/O pin is reset, all pin ports are connected to AF0.

Remapping

Each peripheral has multiple multiplexing functions, but only one multiplexing function input can be selected for a pin, so the multiplexing function of the peripheral can be mapped to other I/O pins, that is, the multiplexing function signal can be reassigned to a pin address.

For details about the pin multiplexing function and remapping address table, see the corresponding data sheet "Port Multiplexing List".

I/O multiplexing configuration

When I/O port is connected to the peripheral multiplexing function, the following debugging needs to be done:

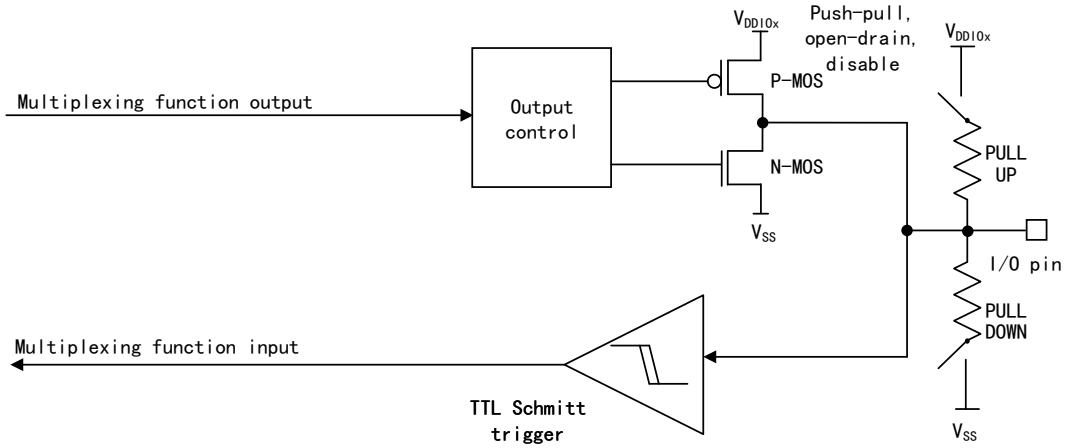
- After reset, the pin is configured with multiplexing function
- I/O port is configured as input, output or analog input
- The I/O port is connected to the defined AFx
- Configure pin pull-up/pull-down and output speed
- Configure I/O as multiplexing function in GPIOx_MODE

When the I/O port is configured with multiplexing function, its input and output mode is as follows:

- Open the output buffer
- Output buffer is driven by peripheral
- Activate schmitt trigger input
- By configuring the pull-up/pull-down register GPIOx_PUPD, select whether to use pull-up/pull-down resistors
- The data on the I/O pin is sampled in each AHB clock cycle and stored in the port input state register
- Read the actual I/O state through the input data register GPIOx_IDATA

The multiplexing mode I/O structure is shown in the figure below:

Figure 21 I/O Structure in Multiplexing Mode



11.4.9 GPIO Locking Function

The locking mechanism of GPIO can protect the configuration of I/O port.Write sequence (specific) to GPIOx_LOCK register so as to freeze the control register of Port A and Port B. If you want to write GPIOx_LOCK register, a specific write/read sequence should be transmitted.I/O configuration can be locked by configuring the lock register (GPIOx_LOCK). When a port bit executes the locking program, the configuration of port bit cannot be modified before the next reset.

11.4.10 HSECLK or LSECLK pin is used as GPIO

By configuring HSEEN/LSEEN in RCM_CTRL1 and RCM_RTCCTRL registers,

set whether to turn on HSECLK/LSECLK RC oscillator.

When HSECLK/LSECLK RC oscillator is turned on, the oscillator controls the related pins, and the related pins are unrelated to GPIO configuration; when HSECLK/LSECLK RC oscillator is turned off, the related oscillators can be used as general GPIO interface.

11.4.11 GPIO is used in RTC power supply domain

When the core power supply domain is powered off, it will lose PC13/PC14/PC15 GPIO function, and at this time, if the configuration of GPIO is not configured by RTC, PC13/14/PC15 pin will be set as analog input mode.

For detailed information about RTC controlled I/O pins, please refer to 20.5.1.

11.5 Register Address Mapping

Table 37 GPIO Register Address Mapping

Register name	Description	Offset address
GPIOx_MODE	Port mode register	0x00
GPIOx_OMODE	Port output mode register	0x04
GPIOx_OSSEL	Port output speed register	0x08
GPIOx_PUPD	Port pull-up/pull-down register	0x0C
GPIOx_IDATA	Port bit input data register	0x10
GPIOx_ODATA	Port bit output data register	0x14
GPIOx_BSC	Port set/reset register	0x18
GPIOx_LOCK	Port lock register	0x1C
GPIOx_ALFL	Port multiplexing function low-8-bit register	0x20
GPIOx_ALFH	Port multiplexing function high-8-bit register	0x24
GPIOx_BR	Port reset register	0x28

11.6 Register Functional Description

11.6.1 Port mode register (GPIOx_MODE) (x=A…D, F)

Offset address: 0x00

Reset value: 0x2800 000 for Port A

0x0000 000 for other ports

Field	Name	R/W	Description
31:0	MODEy[1:0]	R/W	PortxPin y Mode Configure (y=0…15) 00: Input mode (state after reset) 01: Generarl output mode 10: Multiplexing function mode 11: Analog mode

11.6.2 Port output mode register (GPIOx_OMODE) (x=A…D, F)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	OMODEy	R/W	PortxPin y Output Mode Configure (y=0…15) 0: Push-pull output (reset state) 1: Open-drain output
31:16	Reserved		

11.6.3 Port output speed register (GPIOx_OSSEL) (x=A…D, F)

Offset address: 0x08

Reset value: 0x0C00 0000 for Port A

0x0000 000 for other ports

Field	Name	R/W	Description
31:0	OSSELy[1:0]	R/W	PortxPin y Output Speed Select (y=0…15) x0: Low speed 01: Medium speed 11: High speed The speed of configuration I/O port is written by software

11.6.4 Pport pull-up/pull-down register (GPIOx_PUPD) (x=A…D, F)

Offset address: 0x0C

Reset value: 0x2400 000 for Port A

0x0000 000 for other ports

Field	Name	R/W	Description
31:0	PUPDy[1:0]	R/W	PortxPin y Pull-up/Pull-down Configure (y=0…15) These bits are written by software to configure pull-up/pull-down of the port bit 00: Pull-up/Pull-down is disabled 01: Pull up 10: Pull down 11: Reserved

11.6.5 Port bit input data register (GPIOx_IDATA) (x=A..D, F)

Offset address: 0x10

Reset value: 0x0000 XXXX

Field	Name	R/W	Description
15:0	IDATAy	R	PortxPin y Input Data (y=0…15) These bits can only be read to store the input values of the corresponding I/O ports
31:16	Reserved		

11.6.6 Port bit output data register (GPIOx_ODATA) (x=A..D, F)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	ODATAy	R/W	PortxPin y Output Data (y=0…15) Read and write operation can be performed by software For atomic bit setting/setting, the ODATAy bit can be set separately by writing to GPIOx_BSC or GPIOx_BR register
31:16	Reserved		

11.6.7 Port set/reset register (GPIOx_BSC) (x=A…D, F)

Offset address: 0x18

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	BSy	W	PortxPin y Set bit (y=0…15) These bits can only perform write operation, and the value of 0x0000 is returned when reading these bits. These bits are used to affect the corresponding ODATAy bits 0: No effect 1: Set the corresponding ODATAy bit
31:16	BCy	W	PortxPin y Reset Bit (y=0…15) These bits can only perform write operation, and the value of 0x0000 is returned when reading these bits. These bits are used to affect the corresponding ODATAy bits 0: No effect 1: Corresponding ODATAy bit is cleared If BSy bit and BCy bit are set at the same time, BSy has the priority

11.6.8 Port lock register (GPIOx_LOCK) (x=A…B)

This register protects the configuration of GPIO from being modified by mistake during the running of the program. If the GPIO configuration is modified again, it can be modified only after the system is reset. When configuring GPIO locking function, it is necessary to execute the specified sequence to the register to start the GPIO locking function.

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	LOCKy	R/W	PortxLock bit y Configure) (y=0…15) 0: The configuration of Port x Pin y is not locked 1: The configuration of Port x Pin y is locked These bits can be read and written, but can only be written when LOCKKEY=0.
16	LOCKKEY	R/W	LOCK key This bit determines whether the port configuration lock key bit is activated 0: Not activated 1: Activated; GPIOx_LOCK register is locked until the next MUC reset is generated. Lock key write sequence: Write LOCK[16]=1+LOCK[15:0] Write LOCK[16]=0+LOCK[15:0] Write LOCK[16]=1+LOCK[15:0] Read LOCK Read LOCK[16]=1 (this read operation can be selected to confirm whether to activate the lock key) Note: (1) The value of LOCKy cannot be changed during the write sequence of the operation lock key.

Field	Name	R/W	Description
			(2) Any error in the write sequence of operation lock key will abort the lock. (3) After the first lock sequence on any bit of the port, any read access on the LOCKKEY bit will return "1" until the next MCU is reset or the peripheral is reset.
31:17	Reserved		

11.6.9 Port multiplexing function low 8-bit register (GPIOx_ALFL) (x=A…D, F)

Offset address: 0x20

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	ALFSELy	R/W	PortxPin y Alternate Function Select (y=0….7) These bits can be read by software to configure the multiplexing function of the port. ALFSELy selection: 0000:AF0 0001:AF1 0010:AF2 0011:AF3 0100:AF4 0101:AF5 0110:AF6 0111:AF7 1xxx: Reserved

11.6.10 Port multiplexing function high 8-bit register (GPIOx_ALFH) (x=A…D, F)

Offset address: 0x24

Reset value: 0x0000 0000

Field	Name	R/W	Description
31:0	ALFSELy	R/W	PortxPin y Alternate Function Select (y=8….15) These bits can be read by software to configure the multiplexing function of the port. ALFSELy selection: 0000:AF0 0001:AF1 0010:AF2 0011:AF3 0100:AF4 0101:AF5 0110:AF6 0111:AF7 1xxx: Reserved

11.6.11 Port reset register (GPIOx_BR) (x=A…D, F)

Offset address: 0x28

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	BRy	W	PortxPin y Reset Configure (y=0…15) These bits can only perform write operation, and the returned value is 0x0000 when reading these bits. These bits are used to affect the corresponding ODATA 0: No effect 1: Corresponding ODATA bit is cleared
31:16	Reserved		

12 Timer Overview

12.1 Full Name and Abbreviation Description of Terms

Table 38 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Timer	TMR
Update	U
Request	R
Event	EV
Capture	C
Compare	C
Length	LEN

12.2 Timer Category and Main Difference

In this series of products, there are three types of timers: advanced timer, general-purpose timer and basic timer (watchdog timer , System tick timer is described in other chapters).

The advanced timer includes the functions of general-purpose timer and basic timer. The advanced timer has four capture/compare channels, supports timing function, input capture and output compare function, breaking and complementary output function, and is a 16-bit timer that can count up/down.

The function of general-purpose timer is simpler than that of advanced timer. The main differences are the total number of channels, the number of complementary output channel groups and the breaking function.

The basic timer is a timer that can only realize timing function and has no external interface.

The main differences of timers included in the products are shown in the table below:

Table 39 Main Differences among Timers Included in the Products

Item	Specific content/Category	Advanced timer	General-purpose timer				Basic timer
Name	—	TMR1	TMR3	TMR14	TMR15	TMR16/17	TMR6
Timebase unit	Counter	16 bits	16 bits	16 bits	16 bits	16 bits	16 bits
	Prescaler	16 bits	16 bits	16 bits	16 bits	16 bits	16 bits
	Count mode	Up Down Center-aligned	Up Down Center-aligned	Up	Up	Up	Up
Channel	Input channel	4	4	1	2	1	0
	Capture/Compare channel	4	4	1	2	1	0

Item	Specific content/Category	Advanced timer	General-purpose timer				Basic timer
	Output channel	7	4	1	2	1	0
	Complementary output channel	3 groups	0	0	1	1	0
Function	General DMA request	OK	OK	OK	OK	OK	OK
	PWM mode	Yes	Yes	Yes	Yes	None	None
	Single-pulse mode	Yes	Yes	None	Yes	Yes	None
	Forced output mode	Yes	Yes	Yes	Yes	Yes	None
	Dead-time insertion	Yes	None	None	Yes	Yes	None

Timer term

Table 40 Definitions and Terms of Pins

Name	Description
TMRx_ETR	External trigger signal of Timer x
TMRx_CH1、TMRx_CH2、TMRx_CH3、TMRx_CH4	Channel 1/2/3/4 of Timer x
TMRx_CHyN	Complementary output channel y of Timer x
TMRx_BKIN	Breaking signal of Timer x

Table 41 Definitions and Terms of Internal Signals

Name	Description
ETR	TMRx_ETR external trigger signal
ETRF	External trigger filter
ETRP	External trigger prescaler
-	
ITR，ITR0，ITR1	Internal trigger
TRGI	Clock/Trigger/Slave mode controller trigger input
TIF_ED	Timer input filter edge detection
-	
CK_PSC	Prescaler clock
CK_CNT	Counter clock
PSC	Prescaler
CNT	Counter
AUTORLD	Autoload register
-	
TIx，TI1	Timer input

Name	Description
TIxF，TI1F	Timer input filter
TI1_ED	Timer input edge detection
TIxFPx，TI1FP1	Timer input filter polarity
ICx，IC1	Input capture
ICxPS，IC1PS	Input capture prescaler
TRC	Trigger capture
BRK	Breaking signal
-	
OCx，OC1	Timer output coparison channel
OCxREF，OC1REF	Output compare reference signal
-	
TGI	Trigger interrupt
BI	Breaking interrupt
CCxI，CC1I	Capture/Compare interrupt
UEV	Update event
UIFLG	Update interrupt flag

13 Advanced Timer (TMR1)

13.1 Introduction

The advanced timer TMR1 takes the time base unit as the core, and has the functions of input capture, output compare and breaking input, including a 16-bit auto load counter. The advanced timer supports complementary output, repeat count and programmable dead-time insertion function, and is more suitable for motor control.

13.2 Main Characteristics

（1） Timebase unit
- Counter: 16-bit counter, count-up, count-down and center-aligned count
- Prescaler: 16-bit programmable prescaler
- Repeat counter: 16-bit repeat counter
- Auto reloading function

（2） Clock source selection
- Internal clock
- External input
- External trigger
- Internal trigger

（3） Input capture function
- Counting function
- PWM input mode (measurement of pulse width, frequency and duty cycle)
- Encoder interface mode

（4） Output compare function
- PWM output mode
- Forced output mode
- Single-pulse mode
- Complementary output and dead-time insertion

（5） Timing function

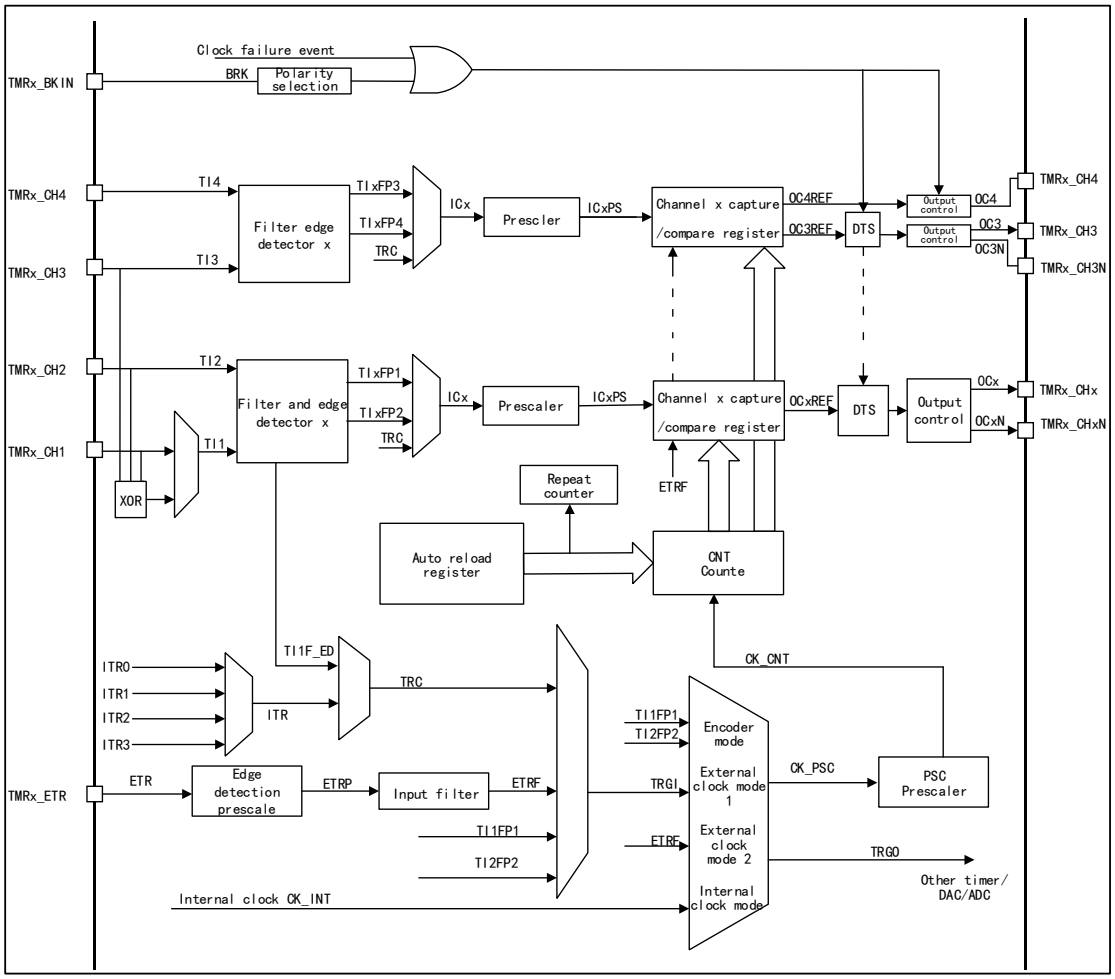
（6） Breaking function

（7） Master/Slave mode controller of timer
- Timers can be synchronized and cascaded
- Support multiple slave modes and synchronization signals

（8） Interrupt output and DMA request event
- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Compare event
- Breaking signal input event

13.3 Structure Block Diagram

Figure 22 TMR1 Structure Block Diagram



13.4 Functional Description

13.4.1 Clock Source Selection

The advanced timer has four clock sources

Internal clock

It is TMR1_CLK from RCM, namely the driving clock of the timer; when the slave mode controller is disabled, the clock source CK_PSC of the prescaler is driven by the internal clock CK_INT.

External clock mode 1

The trigger signal generated from the input channel TI1/2/3/4 of the timer after polarity selection and filtering is connected to the slave mode controller to control the work of the counter. Besides, the pulse signal generated by the input of Channel 1 after double-edge detection of the rising edge and the falling edge is logically equal or the future signal is TI1F_ED signal, namely double-edge signal of TIF_ED. Specially the PWM input can only be input by TI1/2.

External clock mode 2

After polarity selection, frequency division and filtering, the signal from external trigger interface (ETR) is connected to slave mode controller through trigger input selector to control the work of counter.

Internal trigger input

The timer is set to work in slave mode, and the clock source is the output signal of other timers. At this time, the clock source has no filtering, and the synchronization or cascading between timers can be realized. The master mode timer can reset, start, stop or provide clock for the slave mode timer.

13.4.2 Timebase unit

The time base unit in the advanced timer contains four registers

- Counter register (CNT) 16 bits
- Auto reload register (AUTORLD) 16 bits
- Prescaler register (PSC) 16 bits
- Repetition count register (REPCNT) 8 bits

Counter CNT

There are three counting modes for the counter in the advanced timer

- Count-up mode
- Count-down mode
- Center-aligned mode

Count-up mode

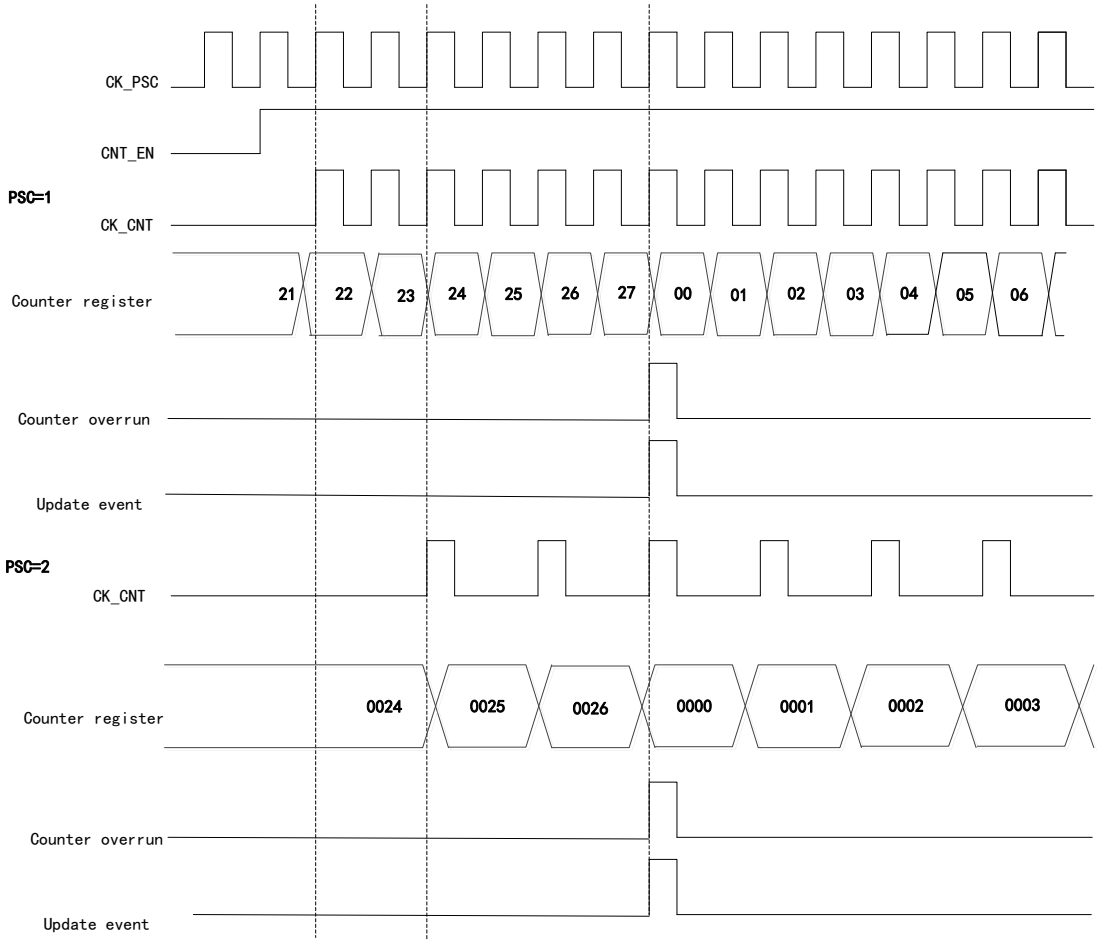
Set to the count-up mode by CNTDIR bit of configuration control register (TMR1_CTRL1).

When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMR1_CNT) is equal to the value of the auto reload (TMR1_AUTORLD), the counter will start to count again from 0, a count-up overrun event will be generated, and the value of the auto reload (TMR1_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the repeat count shadow register, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by UD bit of configuration control register TMR1_CTRL1.

The figure below is Timing Diagram when Division Factor is 1 or 2 in Count-up Mode

Figure 23 Timing Diagram when Division Factor is 1 or 2 in Count-up Mode



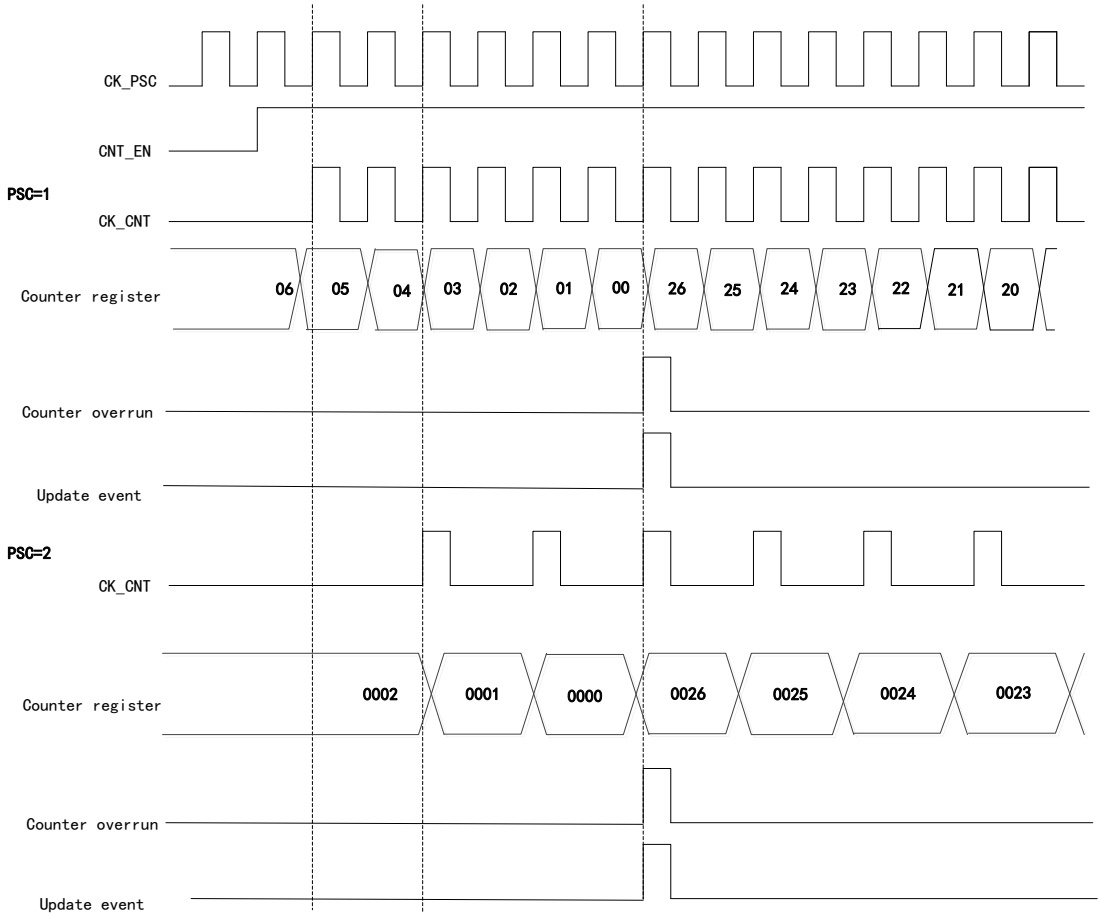
Count-down mode

Set to the count-down mode by CNTDIR bit of configuration control register (TMR1_CTRL1).

When the counter is in count-down mode, the counter will start to count down from the value of the auto reload (TMR1_AUTORLD); every time a pulse is generated, the counter will decrease by 1 and when it becomes 0, the counter will start to count again from (TMR1_AUTORLD), meanwhile, a count-down overrun event will be generated, and the value of the auto reload (TMR1_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the repeat count shadow register, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by configuring the UD bit of the TMR1_CTRL1 register.

Figure 24 Timing Diagram when Division Factor is 1 or 2 in Count-down Mode

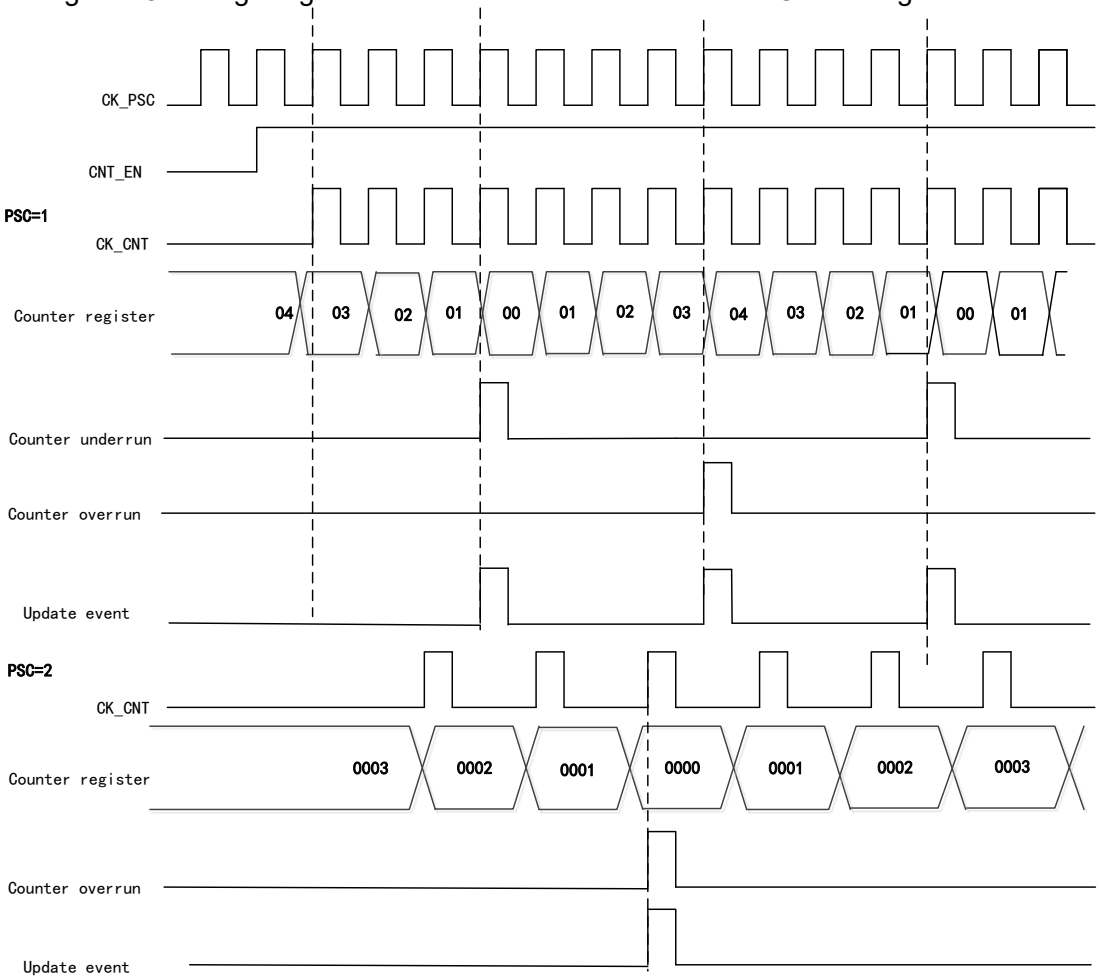


Center-aligned mode

Set to the center-aligned mode by CNTDIR bit of configuration control register (TMR1_CTRL1).

When the counter is in center-aligned mode, the counter counts up from 0 to the value of auto reload (TMR1_AUTORLD), then counts down to 0 from the value of the auto reload (TMR1_AUTORLD), which will repeat; in counting up, when the counter value is (AUTORLD-1), a counter overrun event will be generated; in counting down, when the counter value is 1, a counter underrun event will be generated.

Figure 25 Timing Diagram when Division Factor is 1 or 2 in Center-aligned Mode



Repeatition counter REPCNT

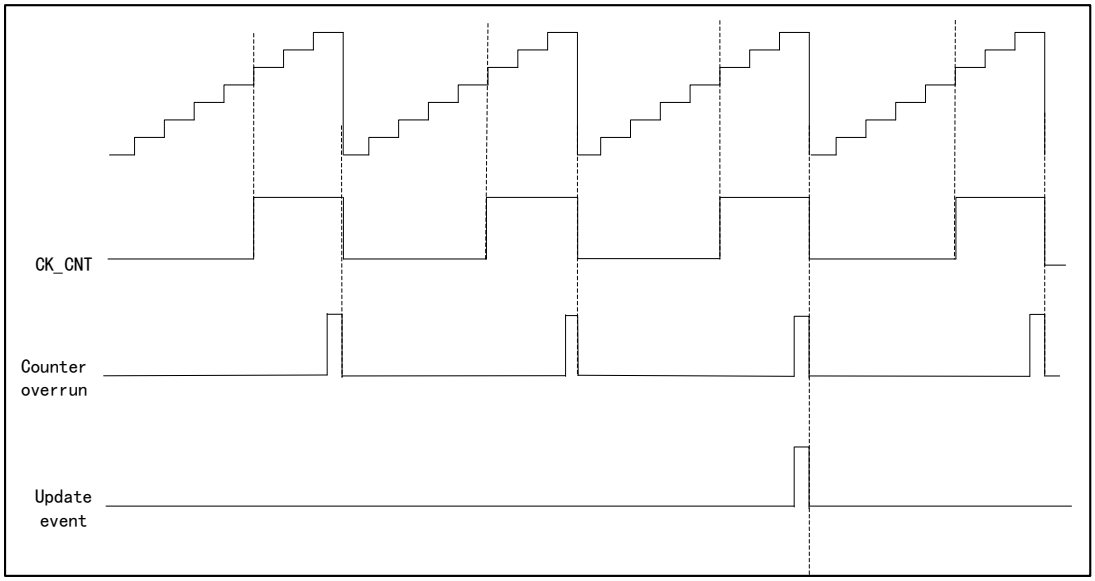
In advanced timer TMR1, because of the existence of repeat counter, when the advanced timer has an up/down overflow event, the update event will be generated only when the repeat counter value is 0.

For example, if the advanced timer needs to generate an update event when an overrun/underrun event occurs, the value of the repeat counter should be set to 0.

If the repeat counter function is used in the count-up mode, every time the counter counts up to AUTORLD, an overrun event will occur. At this time, the value of the repeat counter will be decreased by 1, and an update event will be generated until the value of the repeat counter is 0.

That is, when N+1 (N is the value of repeat counter) overrun/underrun events occur, an update event will be generated.

Figure 26 Timing Diagram when Setting REPCNT=2 in Count-up Mode



Prescaler PSC

The 16-bit programmable prescaler can divide the clock frequency of the counter by any value from 1 to 65536 (controlled by TMR1_PSC register). The clock after frequency division will drive the counter CNT to count.The prescaler has a buffer, which can be changed during running.

13.4.3 Input Capture

Input capture channel

The advanced timer has four independent capture/compare channels, each of which is surrounded by a capture/compare register.

In the input capture, the measured signal will enter from the external pin T1/2/3/4 of the timer, first pass through the edge detector and input filter, and then into the capture channel. Each capture channel has a corresponding capture register. When the capture occurs, the value of the counter CNT will be latched in the capture register CCx. Before entering the capture register, the signal will pass through the prescaler, which is used to set how many events to capture at a time.

Input capture application

Input capture is used to capture external events, and can give the time flag to indicate the occurrence time of the event and measure the pulse jump edge events (measure the frequency or pulse width), for example, if the selected edge appears on the input pin, the TMRx_CCx register will capture the current value of the counter and the CCxIFLG bit of the state register TMRx_STS will be set to 1; if CCxIEN=1, an interrupt will be generated.

In capture mode, the timing, frequency, period and duty cycle of a waveform can

be measured. In the input capture mode, the edge selection is set to rising edge detection. When the rising edge appears on the capture channel, the first capture occurs, at this time, the value of the counter CNT will be latched in the capture register CCx; at the same time, it will enter the capture interrupt, a capture will be recorded in the interrupt service program and the value will be recorded. When the next rising edge is detected, the second capture occurs, the value of counter CNT will be latched in capture register CCx again, at this time, it will enter the capture interrupt again, the value of capture register will be read, and the cycle of this pulse signal will be obtained through capture.

13.4.4 Output Compare

There are eight modes of output compare: freeze, channel x is valid level when matching, channel x is invalid level when matching, flip, force is invalid, force is valid, PWM1 and PWM2 modes, which are configured by OCxMOD bit in TMRx_CCMx register and can control the waveform of output signal in output compare mode.

Output compare application

In the output compare mode, the position, polarity, frequency and time of the pulse generated by the timer can be controlled.

When the value of the counter is equal to that of the capture/compare register, the channel output can be set as high level, low level or flip by configuring the OCxMOD bit in TMRx_CCMx register and the CCxPOL bit in the output polarity TMRx_CCEN register.

When CCxIFLG=1 in TMRx_STS register, if CCxIEN=1 in TMRx_DIEN register, an interrupt will be generated; if CCDSEL=1 in TMRx_CTRL2 register, DMA request will be generated.

13.4.5 PWM Output Mode

PWM mode is an adjustable pulse signal output by the timer. The pulse width of the signal is determined by the value of the compare register CCx, and the cycle is determined by the value of the auto reload AUTORLD.

PWM output mode contains PWM mode 1 and PWM mode 2; PWM mode 1 and PWM mode 2 are divided into count-up, count-down and edge alignment counting; in PWM mode 1, if the value of the counter CNT is less than the value of the compare register CCx, the output level will be valid; otherwise, it will be invalid.

Set the timing diagram in PWM mode 1 when CCx=5, AUTORLD=7

Figure 27 PWM1 Count-up Mode Timing Diagram

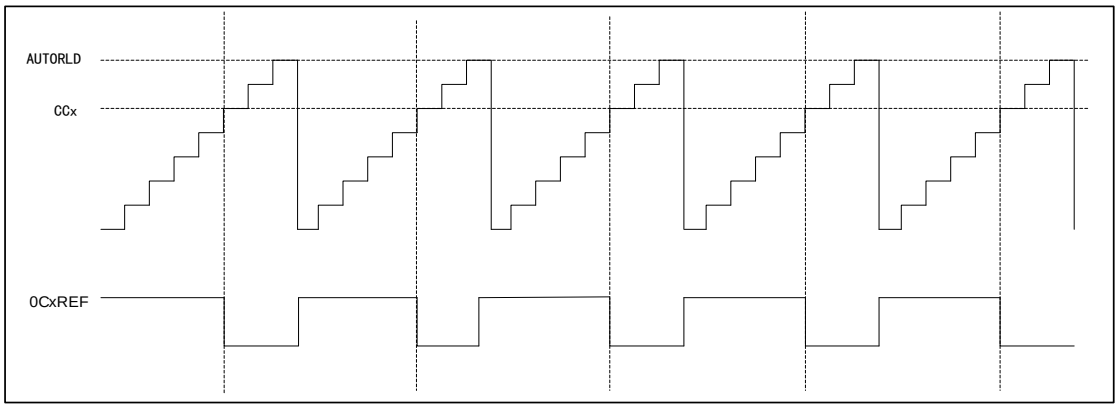


Figure 28 PWM1 Count-down Mode Timing Diagram

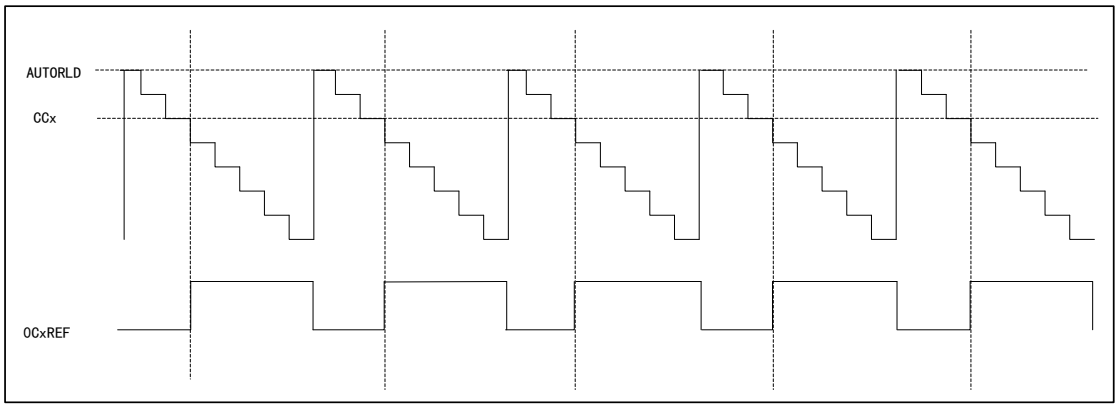
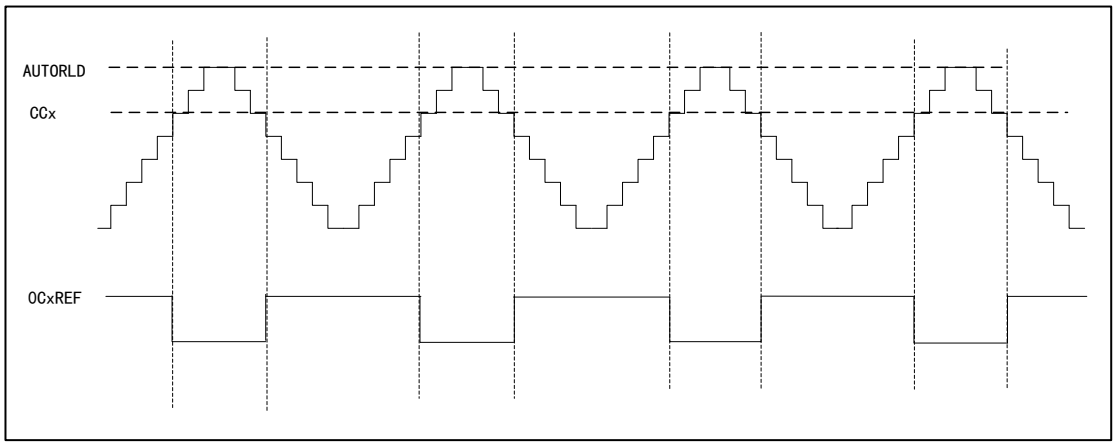


Figure 29 PWM1 Center-aligned Mode Timing Diagram



In PWM mode 2, if the value of the counter CNT is less than that of the compare register CCx, the output level will be invalid; otherwise, it will be valid.

Set the timing diagram in PWM mode 2 when CCx=5, AUTORLD=7

Figure 30 PWM2 Count-up Mode Timing Diagram

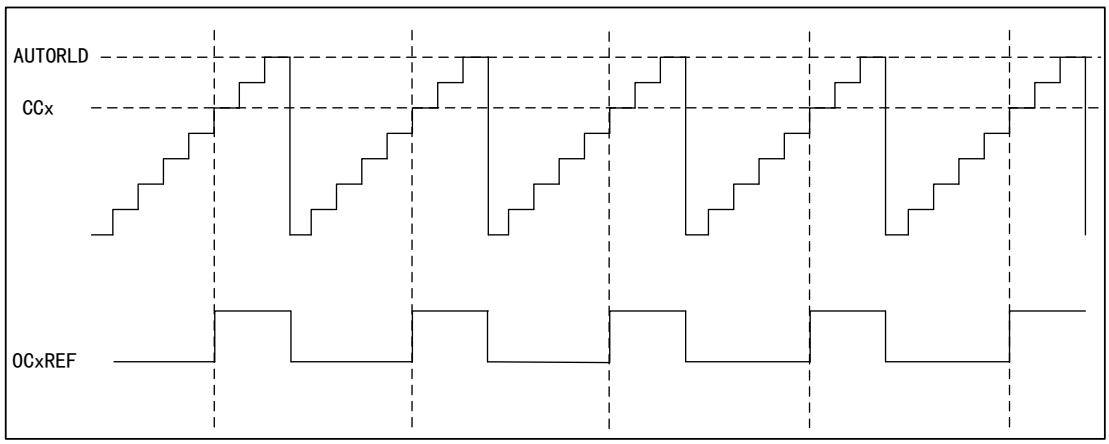


Figure 31 PWM2 Count-down Mode Timing Diagram

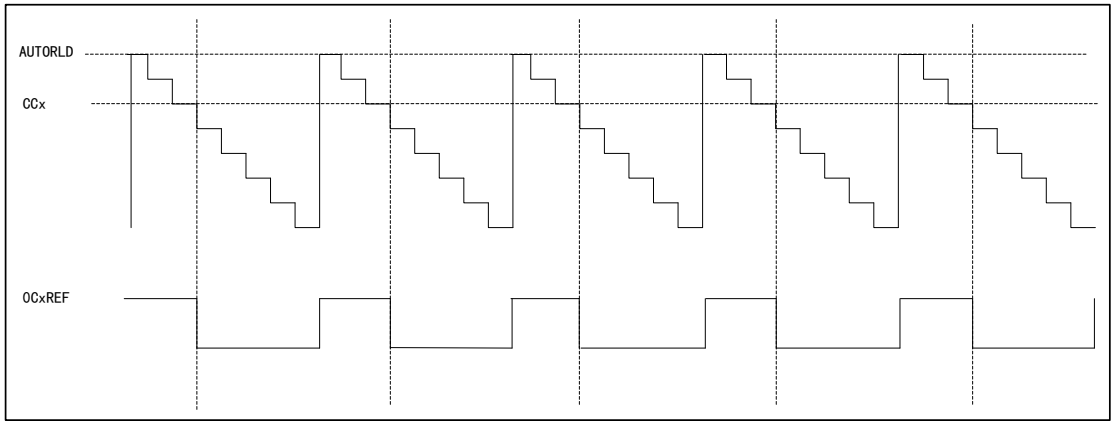
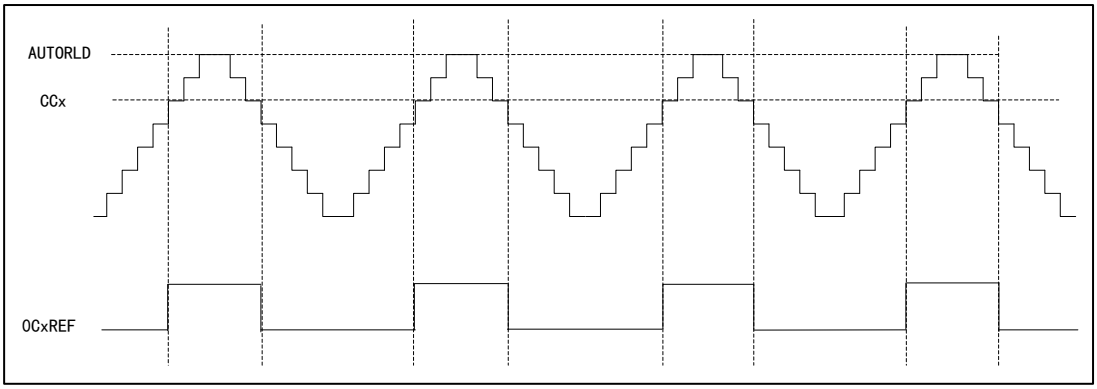


Figure 32 PWM2 Center-aligned Mode Timing Diagram



13.4.6 PWM Input Mode

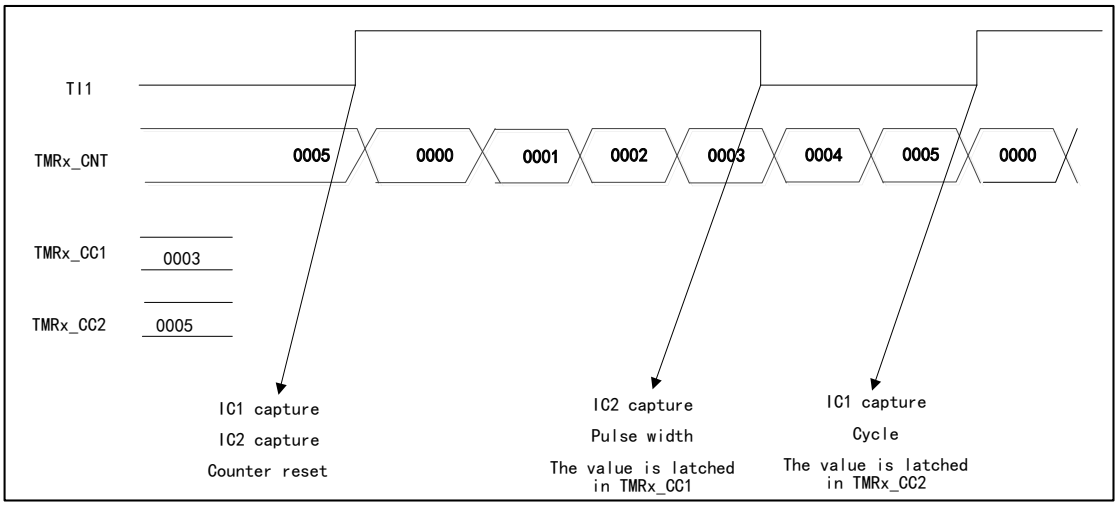
PWM input mode is a particular case of input capture.

In PWM input mode, as only TI1FP1 and TI1FP2 are connected to the slave mode controller, input can be performed only through the channels TMR1_CH1 and TMRx_CH2, which need to occupy the capture registers of CH1 and CH2.In the PWM input mode, the PWM signal enters from TMRx_CH1, and the signal will be divided into two channels, one can measure the cycle and the other can measure

the duty cycle. In the configuration, it is only required to set the polarity of one channel, and the other will be automatically configured with the opposite polarity.

In this mode, the slave mode controller should be configured as the reset mode (SMFSEL bit of TMRx_SMCTRL register).

Figure 33 Timing Diagram in PWM Input Mode



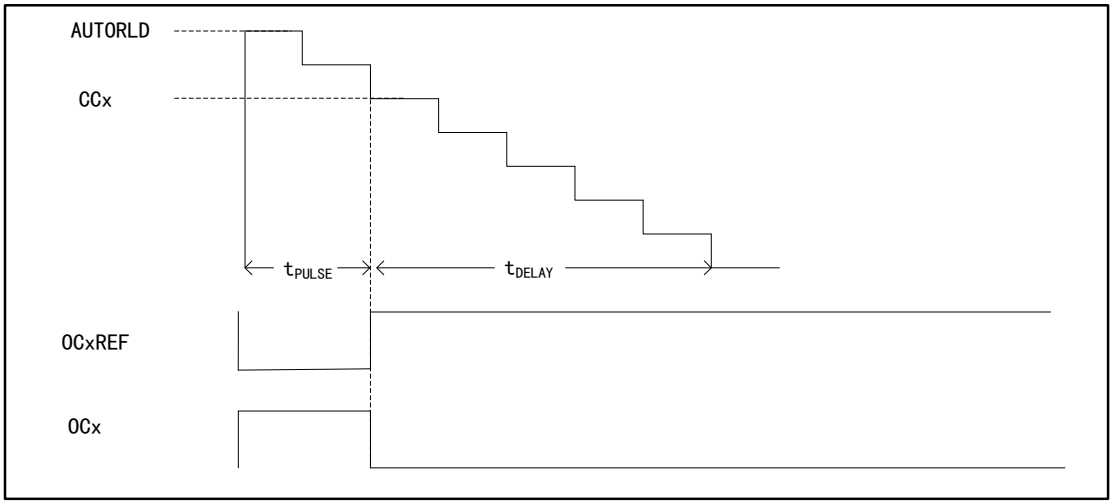
13.4.7 Single-pulse Mode

The single-pulse mode is a special case of timer compare output, and is also a special case of PWM output mode.

Set SPMEN bit of TMR1_CTRL1 register, and select the single-pulse mode. After the counter is started, a certain number of pulses will be output before the update event occurs. When an update event occurs, the counter will stop counting, and the subsequent PWM waveform output will no longer be changed.

After a certain controllable delay, a pulse with controllable pulse width is generated in single-pulse mode through the program. The delay time is defined by the value of TMRx_CCx register; in the count-up mode, the delay time is CCx and the pulse width is AUTORLD-CCx; in the count-down mode, the delay time is AUTORLD-CCx and the pulse width is CCx.

Figure 34 Timing Diagram in Single-pulse Mode



13.4.8 Impact of the Register on Output Waveform

The following registers will affect the level of the timer output waveform. For details, please refer to "Register Functional Description".

（1） CCxEN and CCxNEN bits in TMR1_CCEN register

- CCxNEN=0 and CCxEN=0: The output is turned off (output disabled, invalid state)
- CCxNEN=1 and CCxEN=1: The output is turned on (output enabled, normal output)

（2） MOEN bit in TMRx_BDT register

- MOEN=0: Idle mode
- MOEN=1: Run mode

（3） OCxOIS and OCxNOIS bits in TMR1_CTRL2 register

- OCxOIS=0 amd OCxNOIS=0: When idle (MOEN=0), the output level after the dead-time is 0
- OCxOIS=1 amd OCxNOIS=1: When idle (MOEN=0), the output level after the dead-time is 1

（4） RMOS bit in TMR1_BDT register

- Application environment of RMOS: In corresponding complementary channel and timer run mode (MOEN=1), the timer is not working (CCxEN=0, CCxNEN=0) or is working (CCxEN=1, CCxNEN=1)

（5） IMOS bit in TMR1_BDT register

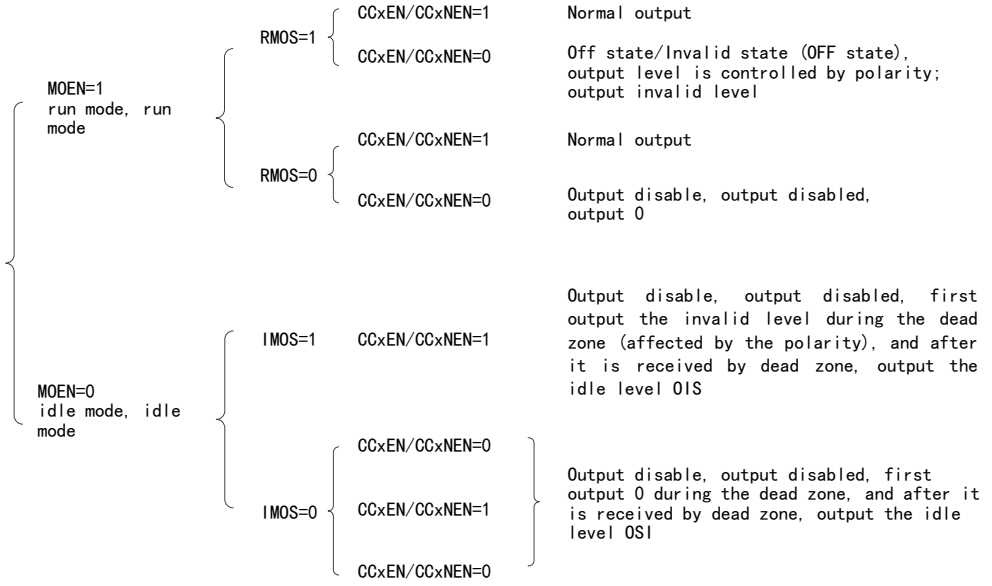
- Application environment of IMOS: In corresponding complementary channel and timer are in idle mode (MOEN=0), the timer is not working (CCxEN=0, CCxNEN=0) or is working (CCxEN=1, CCxNEN=1)

（6） CCxPOL and CCxNPOL bits of TMR1_CCEN register

- CCxPOL=0 and CCxNPOL=0: Output polarity, high level is valid
  CCxPOL=1 and CCxNPOL=1: Output polarity, the low level is valid

The following figure lists the register structure relationships that affect the output waveform

Figure 35 Register Structural Relationship Affecting Output Waveform



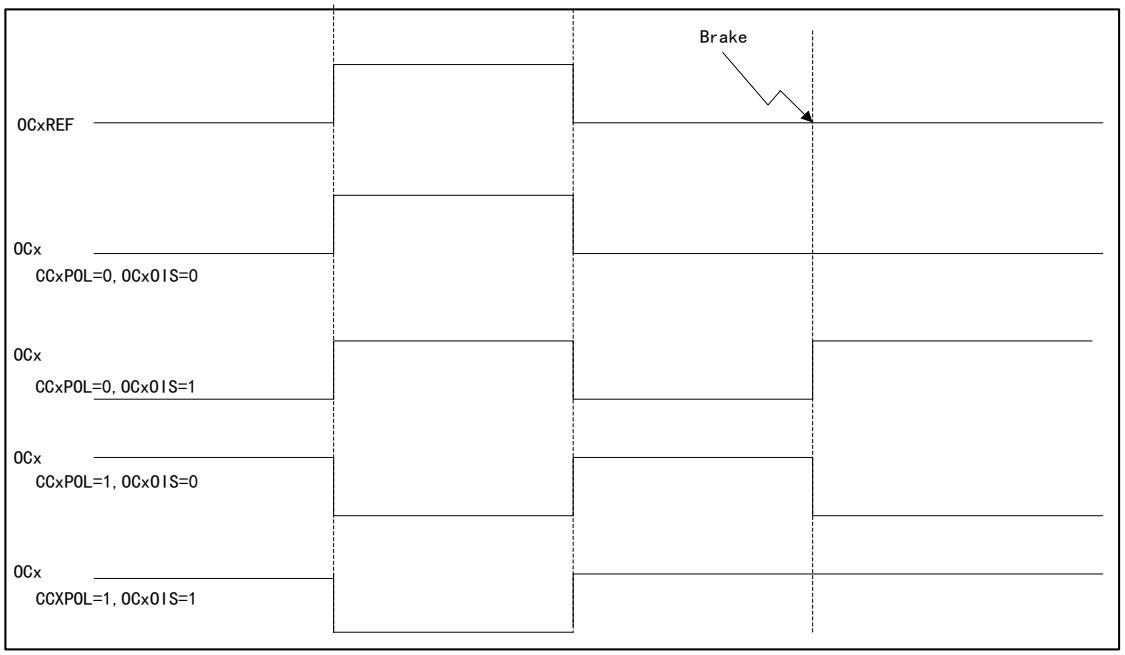
13.4.9 Breaking Function

The signal source of breaking is clock fault event and external input interface.

Besides, the BRKEN bit in TMR1_BDT register can enable the breaking function, and the BRKPOL bit can configure the polarity of breaking input signal.

When a breaking event occurs, the output pulse signal level can be modified according to the state of the relevant control bit.

Figure 36 Breaking Event Timing Diagram

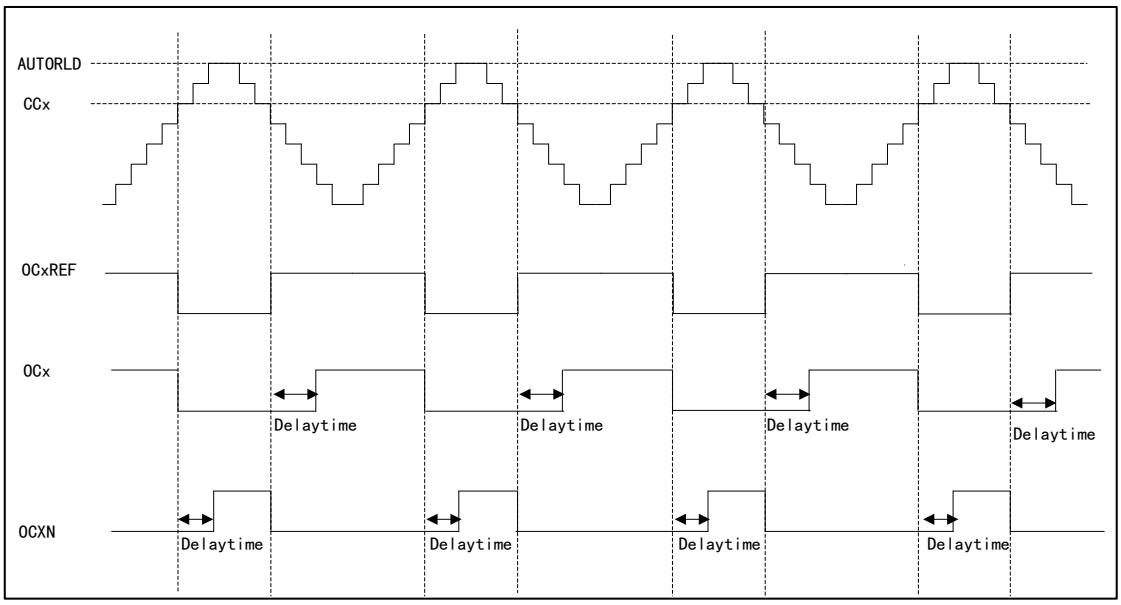


13.4.10 Complementary Output and Dead-time Insertion

TMR 1 timer has three groups of complementary ouptut channels. The insertion dead time is used to generate complementary output signals to ensure that the two-way complementary signals of channels will not be valid at the same time. The dead time is set according to the output device connected to the timer and its characteristics

The duration of the dead-time can be controlled by configuring DTS bit of TMR1_BDT register

Figure 37 Complementary Output of Insertion with Dead-time



13.4.11 Forced Output Mode

In the forced output mode, the compare result is ignored, and the corresponding level is directly output according to the configuration instruction.

- CCxSEL=00 for TMR1_CCMx register, set CCx channel as output
- OCxMOD=100/101 for TMR1_CCMx register, set to force OCxREF signal to invalid/valid state

In this mode, the corresponding interrupt and DMA request will still be generated.

13.4.12 Encoder Interface Mode

The encoder interface mode is equivalent to an external clock with direction selection. In the encoder interface mode, the content of the timer can always indicate the position of the encoder.

The selection methods of encoder interface is as follows:

- By setting SMFSEL bit of TMR1_SMCTRL register, set the counter to count on the edge of TI1 channel /TI2 channel, or count on the edge of TI1 and TI2 at the same time.
- Select the polarity of TI1 and TI2 by setting the CC1POL and CC2POL bits of TMR1_CCEN register.
- Select to filter or not by setting the IC1F and IC2F bits of TMR1_CCM1 register.

The two input TI1 and TI2 can be used as the interface of incremental encoder. The counter is driven by the effective jump of the signals TI1FP1 and TI2FP2 after filtering and edge selection in TI1 and TI2.

The count pulse and direction signal are generated according to the input signals of TI1 and TI2

- The counter will count up/down according to the jumping sequence of the input signal
- Set CNTDIR of control register TMR1_CTRL1 to be read-only (CNTDIR will be re-calculated due to jumping of any input end)

The change mechanism of counter count direction is shown in the figure below

Table 42 Relationship between Count Direction and Encoder

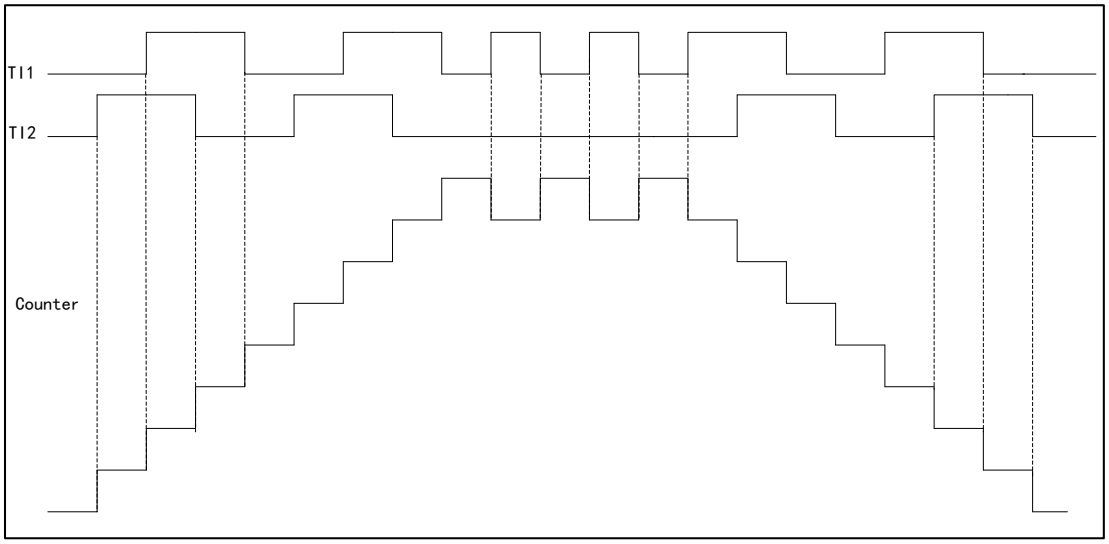
Effective edge		**Count only in TI1**		**Count only in TI2**		**Count in both TI1 and TI2**	
Level of relative signal		High	Low	High	Low	High	Low
TI1FP1	Rising edge	Count down	Count up	—		Count down	Count up
	Falling edge	Count up	Count down			Count up	Count down
TI2FP2	Rising edge	—		Count up	Count down	Count up	Count down
	Falling edge			Count down	Count up	Count down	Count up

The external incremental encoder can be directly connected with MCU, not needing external interface logic, so the comparator is used to convert the differential output of the encoder to digital signal to increase the immunity from noise interference.

Among the following examples,

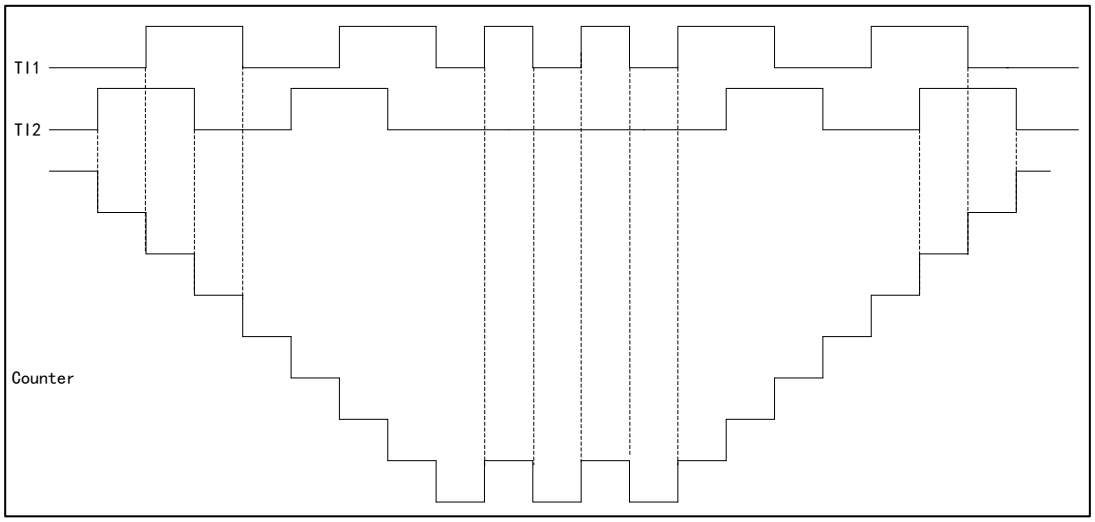
- IC1FP1 is mapped to TI1
- IC2FP2 is mapped to TI2
- Neither IC1FP1 nor IC2FP2 is reverse phase
- The input signal is valid at the rising edge and falling edge
- Enable the counter

Figure 38 Counter Operation Example in Encoder Mode



For example, when TI1 is at low level, and TI2 is in rising edge state, the counter will count up.

Figure 39 Example of Encoder Interface Mode of TI1FP1 Reversed Phase



For example, when TI1 is at low level, and the rising edge of TI2 jumps, the counter will count down.

13.4.13 Slave Mode

TMR1 timer can synchronize external trigger

- Reset mode
- Gated mode
- Trigger mode

SMFSEL bit in TMR1_SMCTRL register can be set to select the mode

SMFSEL=100 set the reset mode, SMFSEL=101 set the gated mode, SMFSEL=110 set the trigger mode.

In the reset mode, when a trigger input event occurs, the counter and prescaler will be initialized, and the rising edge of the selected trigger input (TRGI) will reinitialize the counter and generate a signal to update the register.

In the gated mode, the enable of the counter depends on the high level of the selected input. When the trigger input is high, the clock of the counter will be started. Once the trigger input becomes low, the counter will stop (but not be reset). The start and stop of the counter are controlled.

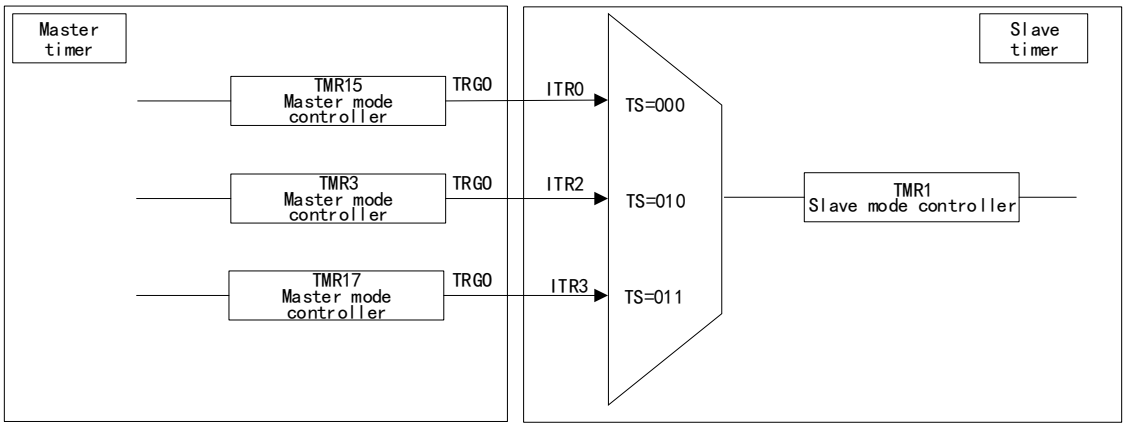
In the trigger mode, the enable of the counter depends on the event on the selected input, the counter is started (but is not reset) at the rising edge of the trigger input, and only the start of the counter is controlled.

13.4.14 Timer Interconnection

Each timer of TMR1 can be connected with each other to realize synchronization or cascading between timers. It is required to configure one timer in master mode and the other timer in slave mode.

When the timer is in master mode, it can reset, start, stop and provide clock source for the counter of the slave mode timer.

Figure 40 Interconnection between TMR1 and Other Timer



Note: The trigger signal for the TMR17 internal connection is TMR17_CH1.

When the timers are interconnected:

- A timer can be used as the prescaler of other register
- Another register can be started by the enable signal of a timer
- Another register can be started by the update event of a timer
- Another register can be selected by the enable of a timer
- Two timers can be synchronized by an external trigger

13.4.15 Interrupt and DMA Request

The timer can generate an interrupt when an event occurs during operation

- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Compare event
- Breaking signal input event.

Some internal interrupt events can generate DMA requests, and special interfaces can enable or disable DMA requests.

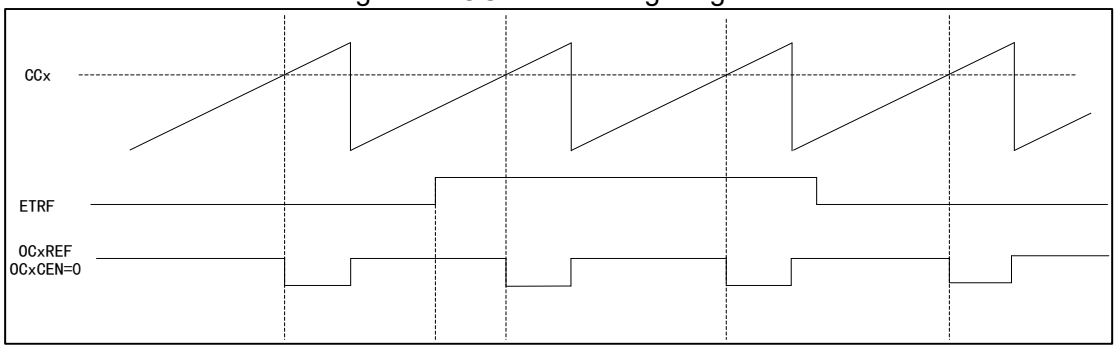
13.4.16 Clear OCxREF signal when external events occur

This function is used for output compare and PWM mode.

In one channel, the high level of ETRF input port will reduce the signal of OCxREF to low level, and the OCxCEN bit in capture/compare register TMR1_CCMx is set to 1, and OCxREF signal will remain low until the next update event.

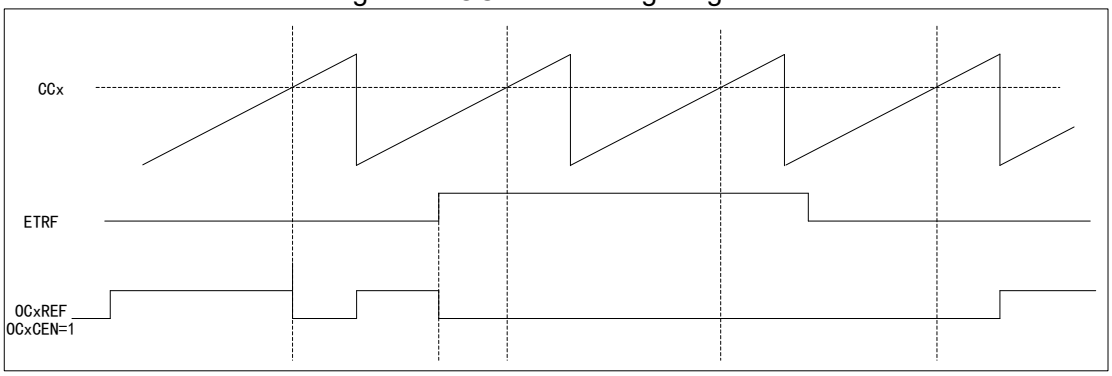
Set TMR1 to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=0, and the output OCxREF signal is shown in the figure below.

Figure 41 OCxREF Timing Diagram



Set TMR1 to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=1, and the output OCxREF signal is shown in the figure below.

Figure 42 OCxREF Timing Diagram



13.5 Register Address Mapping

In the following table, all registers of the advanced timer are mapped to a 16-bit addressable (address) space.

Table 43 TMR1 Register Address Mapping

Register name	Description	Offset address
TMR1_CTRL1	Control register 1	0x00
TMR1_CTRL2	Control register 2	0x04
TMR1_SMCTRL	Slave mode control register	0x08
TMR1_DIEN	DMA/Interrupt enable register	0x0C
TMR1_STS	State register	0x10
TMR1_CEG	Control event generation register	0x14
TMR1_CCM1	Capture/Compare mode register 1	0x18
TMR1_CCM2	Capture/Compare mode register 2	0x1C
TMR1_CCEN	Capture/Compare enable register	0x20
TMR1_CNT	Counter register	0x24
TMR1_PSC	Prescaler register	0x28

Register name	Description	Offset address
TMR1_AUTORLD	Auto reload register	0x2C
TMR1_REPCNT	Repeat count register	0x30
TMR1_CC1	Channel 1 capture/compare register	0x34
TMR1_CC2	Channel 2 capture/compare register	0x38
TMR1_CC3	Channel 3 capture/compare register	0x3C
TMR1_CC4	Channel 4 capture/compare register	0x40
TMR1_BDT	Break and dead-time register	0x44
TMR1_DCTRL	DMA control register	0x48
TMR1_DMADDR	DMA address register of continuous mode	0x4C

13.6 Register Functional Description

13.6.1 Control register 1 (TMR1_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.
1	UD	R/W	Update Disable Update event can cause AUTORLD, PSC and CCx to generate the value of update setting. 0: Update event is allowed (UEV) An update event can occur in any of the following situations: The counter overruns/underruns; Set UEG bit; Update generated by slave mode controller. 1: Update event is disabled
2	URSSEL	R/W	Update Request Source Select If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit. 0: The counter overruns or underruns Set UEG bit Update generated by slave mode controller 1: The counter overruns or underruns
3	SPMEN	R/W	Single Pulse Mode Enable When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed. 0: Disable 1: Enable

Field	Name	R/W	Description
4	CNTDIR	R/W	Counter Direction This bit is read-only when the counter is configured as center-aligned mode or encoder mode. 0: Count up 1: Count down
6:5	CAMSEL	R/W	Center Aligned Mode Select) In the center-aligned mode, the counter counts up and down alternately; otherwise, it will only count up or down. Different center-aligned modes affect the timing of setting the output compare interrupt flag bit of the output channel to 1; when the counter is disabled (CNTEN=0), select the center-aligned mode. 00: Edge alignment mode 01: Center-aligned mode 1 (the output compare interrupt flag bit of output channel is set to 1 when counting down) 10: Center-aligned mode 2 (the output compare interrupt flag bit of output channel is set to 1 when counting up) 11: Center-aligned mode 3 (the output compare interrupt flag bit of output channel is set to 1 when counting up/down)
7	ARPEN	R/W	Auto-reload Preload Enable When the buffer is disabled, the program modification TMR1_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMR1_AUTORLD will modify the values loaded to the counter in the next update event. 0: Disable 1: Enable
9:8	CLKDIV	R/W	Clock Divide Factor For the configuration of dead time and digital filter, CK_INT provides the clock, and the dead time and the clock of the digital filter can be adjusted by setting this bit. 00：$t_{DTS}=t_{CK\_INT}$ 01：$t_{DTS}=2\times t_{CK\_INT}$ 10：$t_{DTS}=4\times t_{CK\_INT}$ 11: Reserved
15:10	Reserved		

13.6.2 Control register 2 (TMR1_CTRL2)

Offset address: 0x04

Reset value: 0x0000

Field	Name	R/W	Description
0	CCPEN	R/W	Capture/Compare Preloaded Enable This bit affects the change of CCxEN, CCxNEN and OCxMOD values. When preloading is disabled, the program modification will immediately affect the timer setting; When preloading is enabled, it is only updated after COMG is set, so as to affect the setting of timer; this bit only works on channels with complementary output. 0: Disable 1: Enable
1	Reserved		
2	CCUSEL	R/W	Capture/compare Control Update Select Only when the capture/compare preload is enabled (CCPEN=1), it works only for complementary output channel. 0: It can only be updated by setting COMG bit 1: It can be updated by setting COMG bit or rising edge on TRGI

Field	Name	R/W	Description
3	CCDSEL	R/W	Capture/compare DMA Select 0: Send DMA request of CCx when CCx event occurs 1: Send DMA request of CCx when an update event occurs
6:4	MMSEL	R/W	Master Mode Signal Select The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with master timer, and specifically affects the configuration of timers in slave mode. 000: Reset; the reset signal of master mode timer is used for TRGO 001: Enable; the counter enable signal of master mode timer is used for TRGO 010: Update; the update event of master mode timer is used for TRGO 011: Comparison pulses; when the master mode timer captures/compares successfully (CCxIFLG=1), a pulse signal is output for TRGO 100: Comparison mode 1; OC1REF is used to trigger TRGO 101: Comparison mode 2; OC2REF is used to trigger TRGO 110: Comparison mode 3; OC3REF is used to trigger TRGO 111: Comparison mode 4; OC4REF is used to trigger TRGO
7	TI1SEL	R/W	Timer Input 1 Select 0: TMR1_CH1 pin is connected to TI1 input 1: TMR1_CH1, TMR1_CH2 and TMR1_CH3 pins are connected to TI1 input after exclusive
8	OC1OIS	R/W	OC1 Output Idle State Configure Only the level state after the dead time of OC1 is affected when MOEN=0 and OC1N is realized. 0：OC1=0 1：OC1=1 Note: When LOCKCFG bit in TMR1_BDT register is at the Level 1, 2 or 3, this bit cannot be modified.
9	OC1NOIS	R/W	OC1N Output Idle State Configure Only the level state after the dead time of OC1 is affected when MOEN=0 and OC1N is realized. 0：OC1N=0 1：OC1N=1 Note: When LOCKCFG bit in TMR1_BDT register is at the Level 1, 2 or 3, this bit cannot be modified.
10	OC2OIS	R/W	Configure OC2 output idle state. Refer to the description of OC1OIS bit
11	OC2NOIS	R/W	Configure OC2N output idle state. Refer to the description of OC1NOIS bit
12	OC3OIS	R/W	Configure OC3 output idle state. Refer to the description of OC1OIS bit
13	OC3NOIS	R/W	Configure OC3N output idle state. Refer to the description of OC1NOIS bit
14	OC4OIS	R/W	Configure OC4 output idle state. Refer to the description of OC1OIS bit
15	Reserved		

13.6.3 Slave mode control register (TMR1_SMCTRL)

Offset address: 0x08

Reset value: 0x0000

Field	Name	R/W	Description
2:0	SMFSEL	R/W	Slave Mode Function Select 000: Disable the slave mode, the timer can be used as master mode timer to affect the work of slave mode timer; if CTRL1_CNTEN=1, the prescaler is directly driven by the internal clock. 001: Encoder mode 1; according to the level of TI1FP1, the counter counts at the edge of TI2FP2.

Field	Name	R/W	Description
			010: Encoder mode 2; according to the level of TI2FP2, the counter counts at the edge of TI1FP1. 011: Encoder mode 3; according to the input level of another signal, the counter counts at the edge of TI1FP1 and TI2FP2. 100: Reset mode; the slave mode timer resets the counter after receiving the rising edge signal of TRGI and generates the signal to update the register. 101: Gated mode; the slave mode timer starts the counter to work after receiving the TRGI high level signal; it stops the counter when receiving TRGI low level; when receiving TRGI high level signal again, the timer will continue to work; the counter is not reset during the whole period. 110: Trigger mode, the slave mode timer starts the counter to work after receiving the rising edge signal of TRGI. 111: External clock mode 1; select the rising edge signal of TRGI as the clock source to drive the counter to work.
3	OCCSEL	R/W	OCREF Clear Source Select This bit is used to select OCREF clear source 0：OCREF_CLR 1：ETRF
6:4	TRGSEL	R/W	Trigger Input Signal Select In order to avoid false edge detection when changing the bit value, it must be changed when SMFSEL=0. 000: Internal trigger ITR0 001: Reserved 010: Internal trigger ITR2 011: Reserved 100: Channel 1 input edge detector TIF_ED 101: Channel 1 post-filtering timer input TI1FP1 110: Channel 2 post-filtering timer input TI2FP2 111: External trigger input (ETRF)
7	MSMEN	R/W	Master/slave Mode Enable 0: Invalid 1: Enable the master/slave mode
11:8	ETFCFG	R/W	External Trigger Filter Configure 0000: Filter disabled, sampling by f_{DTS} 0001：DIV=1，N=2 0010：DIV=1，N=4 0011：DIV=1，N=8 0100：DIV=2，N=6 0101：DIV=2，N=8 0110：DIV=4，N=6 0111：DIV=4，N=8 1000：DIV=8，N=6 1001：DIV=8，N=8 1010：DIV=16，N=5 1011：DIV=16，N=6 1100：DIV=16，N=8

Field	Name	R/W	Description
			1101：DIV=32，N=5 1110：DIV=32，N=6 1111：DIV=32，N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, and a jump is generated by every N events.
13:12	ETPCFG	R/W	External Trigger Prescaler Configure The ETR (external trigger input) signal becomes ETRP after frequency division. The signal frequency of ETRP is at most 1/4 of TMR1CLK frequency; when ETR frequency is too high, the ETRP frequency must be reduced through frequency division. 00: The prescaler is disabled; 01: ETR signal 2 divided frequency 10: ETR signal 4 divided frequency 11: ETR signal 8 divided frequency
14	ECEN	R/W	External Clock Enable Mode2 0: Disable 1: Enable Setting ECEN bit has the same function as selecting external clock mode 1 to connect TRGI to ETRF; slave mode (reset, gating, trigger) can be used at the same time with external clock mode 2, but TRGI cannot be connected to ETRF in such case; when external clock mode 1 and external clock mode 2 are enabled at the same time, the input of external clock is ETRF.
15	ETPOL	R/W	External Trigger Polarity Configure This bit decides whether the external trigger ETR is reversed. 0: The external trigger ETR is not reversed,and the high level or rising edge is valid 1: The external trigger ETR is reversed, and the low level or falling edge is valid

Table 44 TMR1 Internal Trigger Connection

Slave timer	ITR0（TS=000）	ITR2（TS=010）
TMR1	TMR15	TMR3

13.6.4 DMA/Interrupt enable register (TMR1_DIEN)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
0	UIEN	R/W	Update interrupt Enable 0: Disable 1: Enable
1	CC1IEN	R/W	Capture/Compare Channel1 Interrupt Enable 0: Disable 1: Enable
2	CC2IEN	R/W	Capture/Compare Channel2 Interrupt Enable 0: Disable 1: Enable

Field	Name	R/W	Description
3	CC3IEN	R/W	Capture/Compare Channel3 Interrupt Enable 0: Disable 1: Enable
4	CC4IEN	R/W	Capture/Compare Channel4 Interrupt Enable 0: Disable 1: Enable
5	COMIEN	R/W	COM Interrupt Enable 0: Disable 1: Enable
6	TRGIEN	R/W	Trigger interrupt Enable 0: Disable 1: Enable
7	BRKIEN	R/W	Break interrupt Enable 0: Disable 1: Enable
8	UDIEN	R/W	Update DMA Request Enable 0: Disable 1: Enable
9	CC1DEN	R/W	Capture/Compare Channel1 DMA Request Enable 0: Disable 1: Enable
10	CC2DEN	R/W	Capture/Compare Channel2 DMA Request Enable 0: Disable 1: Enable
11	CC3DEN	R/W	Capture/Compare Channel3 DMA Request Enable 0: Disable 1: Enable
12	CC4DEN	R/W	Capture/Compare Channel4 DMA Request Enable 0: Disable 1: Enable
13	COMDEN	R/W	COM DMA Request Enable 0: Disable 1: Enable
14	TRGDEN	R/W	Trigger DMA Request Enable 0: Disable 1: Enable
15	Reserved		

13.6.5 State register (TMR1_STS)

Offset address: 0x10

Reset value: 0x0000

Field	Name	R/W	Description
0	UIFLG	RC_W0	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur 1: Update event interrupt occurs

Field	Name	R/W	Description
			When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations: (1) UD=0 on TMR1_CTRL1 register, and when the value of the repeat counter overruns/underruns, an update event will be generated; (2) URSSEL=0 and UD=0 on TMR1_CTRL1 register, configure UEG=1 on TMR1_CEG register to generate update event, and the counter needs to be initialized by software; (3) URSSEL=0 and UD=0 on TMR1_CTRL1 register, generate update event when the counter is initialized by trigger event.
1	CC1IFLG	RC_W0	Capture/Compare Channel1 Interrupt Flag **When the capture/compare channel 1 is configured as output:** 0: No matching occurred 1: The value of TMR1_CNT matches the value of TMR1_CC1 **When the capture/compare channel 1 is configured as input:** 0: Input capture did not occur 1: Input capture occurred When capture event occurs, the bit is set to 1 by hardware, and it can be cleared by software or cleared when reading TMR1_CC1 register.
2	CC2IFLG	RC_W0	Captuer/Compare Channel2 Interrupt Flag Refer to the description of STS_CC1IFLG
3	CC3IFLG	RC_W0	Capture/Compare Channel3 Interrupt Flag Refer to the description of STS_CC1IFLG
4	CC4IFLG	RC_W0	Captuer/Compare Channel4 Interrupt Flag Refer to the description of STS_CC1IFLG
5	COMIFLG	RC_W0	COM Event Interrupt Generate Flag 0: COM event does not occur 1: COM interrupt waits for response After COM event is generated, this bit is set to 1 by hardware and cleared by software.
6	TRGIFLG	RC_W0	Trigger Event Interrupt Generate Flag 0: Trigger event interrupt did not occur 1: Trigger event interrupt occurred After Trigger event is generated, this bit is set to 1 by hardware and cleared by software.
7	BRKIFLG	RC_W0	Break Event Interrupt Generate Flag 0: Break event does not occur 1: Break event occurs When break input is valid, this bit is set to 1 by hardware; when break input is invalid, this bit can be cleared by software.
8	Reserved		
9	CC1RCFLG	RC_W0	Capture/compare Channel1 Repetition Capture Flag 0: Repeat capture does not occur 1: Repeat capture occurs The value of the counter is captured to TMR1_CC1 register, and CC1IFLG=1; this bit is set to 1 by hardware and cleared by software only when the channel is configured as input capture.
10	CC2RCFLG	RC_W0	Capture/compare Channel2 Repetition Capture Flag Refer to the description of STS_CC1RCFLG
11	CC3RCFLG	RC_W0	Capture/compare Channel3 Repetition Capture Flag Refer to the description of STS_CC1RCFLG
12	CC4RCFLG	RC_W0	Capture/compare Channel4 Repetition Capture Flag Refer to the description of STS_CC1RCFLG
15:13	Reserved		

13.6.6 Control event generation register (TMR1_CEG)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared by hardware. Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMR1_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared.
1	CC1EG	W	Capture/Compare Channel1 Event Generation 0: Invalid 1: Capture/Compare event is generated This bit is set to 1 by software and cleared automatically by hardware. **If Channel 1 is in output mode** When CC1IFLG=1, if CC1IEN and CC1DEN bits are set, the corresponding interrupt and DMA request will be generated. **If Channel 1 is in input mode** The value of the capture counter is stored in TMR1_CC1 register; configure CC1IFLG=1, and if CC1IEN and CC1DEN bits are also set, the corresponding interrupt and DMA request will be generated; at this time, if CC1IFLG=1, it is required to configure CC1RCFLG=1.
2	CC2EG	W	Capture/Compare Channel2 Event Generation Refer to the description of CC1EG description
3	CC3EG	W	Capture/Compare Channel3 Event Generation Refer to the description of CC1EG description
4	CC4EG	W	Capture/Compare Channel4 Event Generation Refer to the description of CC1EG description
5	COMG	W	Capture/Compare Control Update Event Generate 0: Invalid 1: Capture/Compare update event is generated This bit is set to 1 by software and cleared automatically by hardware. Note: COMG bit is valid only in complementary output channel.
6	TEG	W	Trigger Event Generate 0: Invalid 1: Trigger event is generated This bit is set to 1 by software and cleared automatically by hardware.
7	BEG	W	Break Event Generate 0: Invalid 1: Break event is generated This bit is set to 1 by software and cleared automatically by hardware.
15:8	Reserved		

13.6.7 Capture/Compare mode register 1 (TMR1_CCM1)

Offset address: 0x18

Reset value: 0x0000

The timer can be configured as input (capture mode) or output (compare mode) by CCxSEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output mode and input mode. The OCxx in the register describes the function of the channel in the output mode, and the ICxx in the register describes the function of the channel in the input mode.

Output compare mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select This bit defines the input/output direction and the selected input pin. 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR1_CCEN register CC1EN=0).
2	OC1FEN	R/W	Output Compare Channel1 Fast Enable 0: Disable 1: Enable This bit is used to improve the response of the capture/compare output to the trigger input event.
3	OC1PEN	R/W	Output Compare Channel1 Preload Enable 0: Preloading function is disabled; write the value of TMR1_CC1 register through the program and it will work immediately. 1: Preloading function is enabled; write the value of TMR1_CC1 register through the program and it will work after an update event is generated. Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain.
6:4	OC1MOD	R/W	Output Compare Channel1 Mode Configure 000: Freeze The output compare has no effect on OC1REF 001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture/compareregister, OC1REF will be forced to be at high level 010: The output value is low when matching. When the value of the counter matches the value of the capture/compareregister, OC1REF will be forced to be at low level 011: Output flaps when matching. When the value of the counter matches the value of the capture/compareregister, flap the level of OC1REF 100: The output is forced to be ow Force OC1REF to be at low level 101: The output is forced to be high. Force OC1REF to be at high level 110: PWM mode 1 (set to high when the counter value<output compare value; otherwise, set to low) 111: PWM mode 2 (set to high when the counter value>output compare value; otherwise, set to low) Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the compare result changes or when the output compare mode changes from freeze mode to PWM mode.
7	OC1CEN	R/W	Output Compare Channel1 Clear Enable

Field	Name	R/W	Description
			0: OC1REF is unaffected by ETRF input. 1: When high level of ETRF input is detected, OC1REF=0
9:8	CC2SEL	R/W	Capture/Compare Channel2 Select This bit defines the input/output direction and the selected input pin. 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI2 10: CC2 channel is input, and IC2 is mapped on TI1 11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR1_CCEN register CC2EN=0).
10	OC2FEN	R/W	Output Compare Channel2 Preload Enable Refer to the description of OC1FEN description
11	OC2PEN	R/W	Output Compare Channel2 Buffer Enable Refer to the description of OC1PEN description
14:12	OC2MOD	R/W	Output Compare Channel1 Mode Refer to the description of OC1MOD description
15	OC2CEN	R/W	Output Compare Channel2 Clear Enable Refer to the description of OC1CEN description

Input capture mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR1_CCEN bit CC1EN=0).
3:2	IC1PSC	R/W	Input Capture Channel 1 Perscaler Configure 00：PSC=1 01：PSC=2 10：PSC=4 11：PSC=8 PSC is prescaled factor, which triggers capture once every PSC events.
7:4	IC1F	R/W	Input Capture Channel 1 Filter Configure 0000: Filter disabled, sampling by f_{DTS} 0001：DIV=1，N=2 0010：DIV=1，N=4 0011：DIV=1，N=8 0100：DIV=2，N=6 0101：DIV=2，N=8 0110：DIV=4，N=6 0111：DIV=4，N=8 1000：DIV=8，N=6 1001：DIV=8，N=8 1010：DIV=16，N=5 1011：DIV=16，N=6 1100：DIV=16，N=8

Field	Name	R/W	Description
			1101：DIV=32，N=5 1110：DIV=32，N=6 1111：DIV=32，N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events.
9:8	CC2SEL	R/W	Capture/Compare Channel 2 Select 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI2 10: CC2 channel is input, and IC2 is mapped on TI1 11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR1_CCEN register CC2EN=0).
11:10	IC2PSC	R/W	Input Capture Channel 2 Perscaler Configure Refer to the description of IC1PSC description.
15:12	IC2F	R/W	Input Capture Channel 2 Filter Configure Refer to the description of IC1F description.

13.6.8 Capture/Compare mode register 2 （TMR1_CCM2）

Offset address: 0x1C

Reset value: 0x0000

Refer to the description of the above CCM1 register.

Output compare mode:

Field	Name	R/W	Description
1:0	CC3SEL	R/W	Capture/Compare Channel 1 Select This bit defines the input/output direction and the selected input pin. 00: CC3 channel is output 01: CC3 channel is input, and IC3 is mapped on TI3 10: CC3 channel is input, and IC3 is mapped on TI4 11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR1_CCEN register CC3EN=0).
2	OC3FEN	R/W	Output Compare Channel3 Fast Enable 0: Disable 1: Enable This bit is used to improve the response of the capture/compare output to the trigger input event.
3	OC3PEN	R/W	Output Compare Channel3 Preload Enable Refer to the description of OC1PEN description.
6:4	OC3MOD	R/W	Output Compare Channel3 Mode Configure Refer to the description of OC1MOD description.
7	OC3CEN	R/W	Output Compare Channel3 Clear Enable Refer to the description of OC1CEN description.
9:8	CC4SEL	R/W	Capture/Compare Channel 4 Select This bit defines the input/output direction and the selected input pin. 00: CC4 channel is output 01: CC4 channel is input, and IC4 is mapped on TI4 10: CC4 channel is input, and IC4 is mapped on TI3 11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR1_CCEN register CC4EN=0).
10	OC4FEN	R/W	Output Compare Channel4 Preload Enable Refer to the description of OC1FEN description.

Field	Name	R/W	Description
11	OC4PEN	R/W	Output Compare Channel4 Buffer Enable Refer to the description of OC1PEN description.
14:12	OC4MOD	R/W	Output Compare Channel4 Mode Configure Refer to the description of OC1MOD description.
15	OC4CEN	R/W	Output Compare Channel4 Clear Enable Refer to the description of OC1CEN description.

Input capture mode

Field	Name	R/W	Description
1:0	CC3SEL	R/W	Capture/Compare Channel 3 Select 00: CC3 channel is output 01: CC3 channel is input, and IC3 is mapped on TI3 10: CC3 channel is input, and IC3 is mapped on TI4 11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR1_CCEN register CC3EN=0).
3:2	IC3PSC	R/W	Input Capture Channel 3 Perscaler Configure Refer to the description of IC1PSC description.
7:4	IC3F	R/W	Input Capture Channel 3 Filter Configure Refer to the description of IC1F description.
9:8	CC4SEL	R/W	Capture/Compare Channel 4 Select 00: CC4 channel is output 01: CC4 channel is input, and IC4 is mapped on TI4 10: CC4 channel is input, and IC4 is mapped on TI3 11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR1_CCEN register CC4EN=0).
11:10	IC4PSC	R/W	Input Capture Channel 4 Perscaler Configure Refer to the description of IC1PSC description.
15:12	IC4F	R/W	Input Capture Channel 4 Filter Configure Refer to the description of IC1F description.

13.6.9 Capture/Compare enable register (TMR1_CCEN)

Offset address: 0x20

Reset value: 0x0000

Field	Name	R/W	Description
0	CC1EN	R/W	Capture/Compare Channel1 Output Enable **When the capture/compare channel 1 is configured as output:** 0: Output is disabled 1: Output is enabled **When the capture/compare channel 1 is configured as input:** This bit determines whether the value CNT of the counter can be captured and enter TMR1_CC1 register 0: Capture is disabled 1: Capture is enabled
1	CC1POL	R/W	Capture/Compare Channel1 Output Polarity Configure

Field	Name	R/W	Description
			When CC1 channel is configured as output: 0: OC1 high level is valid 1: OC1 low level is valid **When CC1 channel is configured as input:** CC1POL and CC1NPOL control the polarity of the triggered or captured signals TI1FP1 and TI2FP1 at the same time 00: Non-phase-inverting/rising edge: TIxFP1 is not reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode). 01: Inverted phase/Falling edge: TIxFP1 is reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode). 10: Reserved 11: Non-phase-inverting/Rising and falling edges: TIxFP1 is not reversed phase (triggered in gated mode, cannot be used in encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode).
2	CC1NEN	R/W	Capture/Compare Channel1 Complementary Output Enable 0: Disable 1: Enable
3	CC1NPOL	R/W	Capture/Compare Channel1 Complementary Output Polarity **When CC1 channel is configured as output** 0: OC1N high level is valid 1: OC1N low level is valid **When CC1 channel is configured as input** This bit, together with CC1POL, is used to define the polarity of TI1FP1 and TI2FP1 Note: (1) On the complementary output channel, if this bit is preloaded, and CCPEN=1 for TMR1_CTRL2, CC1NPOL can obtain new value from the preload bit only when reversing event is generated. (2) When the protection level is 2 or 3, this bit cannot be modified
4	CC2EN	R/W	Capture/Compare Channel2 Output Enable Refer to the description of CCEN_CC1EN
5	CC2POL	R/W	Capture/Compare Channel2 Output Polarity Configure Refer to the description of CCEN_CC1POL
6	CC2NEN	R/W	Capture/Compare Channel1 Complementary Output Enable Refer to the description of CCEN_CC1NEN
7	CC2NPOL	R/W	Capture/Compare Channel2 Complementary Output Polarity Configure Refer to the description of CCEN_CC1NPOL
8	CC3EN	R/W	Capture/Compare Channel3 Output Enable Refer to the description of CCEN_CC1EN
9	CC3POL	R/W	Capture/Compare Channel3 Output Polarity Configure Refer to the description of CCEN_CC1POL
10	CC3NEN	R/W	Capture/Compare Channel3 Complementary Output Enable

Field	Name	R/W	Description
			Refer to the description of CCEN_CC1NEN
11	CC3NPOL	R/W	Capture/Compare Channel3 Complementary Output Polarity Configure Refer to the description of CCEN_CC1NPOL
12	CC4EN	R/W	Capture/Compare Channel4 Output Enable Refer to the description of CCEN_CC1EN
13	CC4POL	R/W	Capture/Compare Channel4 Output Polarity Refer to the description of CCEN_CC1POL
15:14	Reserved		

13.6.10 Counter register (TMR1_CNT)

Offset address: 0x24

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CNT	R/W	Counter Value

13.6.11 Prescaler register (TMR1_PSC)

Offset address: 0x28

Reset value: 0x0000

Field	Name	R/W	Description
15:0	PSC	R/W	Prescaler Value Clock frequency of counter (CK_CNT)=f_{CK_PSC}/(PSC+1)

13.6.12 Auto reload register (TMR1_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF

Field	Name	R/W	Description
15:0	AUTORLD	R/W	Auto Reload Value When the value of auto reload is empty, the counter will not count.

13.6.13 Repeat count register (TMR1_REPCNT)

Offset address: 0x30

Reset value: 0x0000

Field	Name	R/W	Description
7:0	REPCNT	R/W	Repetition Counter Value When the count value of the repeat counter is reduced to 0, an update event will be generated, and the counter will start counting again from the REPCNT value; the new value newly written to this register is valid only when an update event occurs in next cycle.
15:8	Reserved		

13.6.14 Channel 1 capture/compare register (TMR1_CC1)

Offset address: 0x34

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC1	R/W	Capture/Compare Channel 1 Value **When the capture/compare channel 1 is configured as input mode:** CC1 contains the counter value transmitted by the last input capture channel 1 event. **When the capture/compare channel 1 is configured as output mode:** CC1 contains the current load capture/compare register value. Compare the value CC1 of the capture and compare channel 1 with the value CNT of the counter to generate the output signal on OC1. When the output compare preload is disabled (OC1PEN=0 for TMR1_CCM1 register), the written value will immediately affect the output compare results; If the output compare preload is enabled (OC1PEN=1 for TMR1_CCM1 register), the written value will affect the output compare result when an update event is generated.

13.6.15 Channel 2 capture/compare register (TMR1_CC2)

Offset address: 0x38

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC2	R/W	Capture/Compare Channel 2 Value Refer to TMR1_CC1

13.6.16 Channel 3 capture/compare register (TMR1_CC3)

Offset address: 0x3C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC3	R/W	Capture/Compare Channel 3 Value Refer to TMR1_CC1

13.6.17 Channel 4 capture/compare register (TMR1_CC4)

Offset address: 0x40

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC4	R/W	Capture/Compare Channel 4 Value Refer to TMR1_CC1

13.6.18 Break and dead-time register (TMR1_BDT)

Offset address: 0x44

Reset value: 0x0000

Note: According to the lock setting, AOEN, BRKPOL, BRKEN, IMOS, RMOS and DTS[7:0] bits all can be write-protected, and it is necessary to configure them when writing to TMR1_BDT register for the first time.

Field	Name	R/W	Description
7:0	DTS	R/W	Dead Time Setup DT is the dead duration, and the relationship between DT and register DTS is as follows: DTS[7:5]=0xx=>DT=DTS[7:0]×T_{DTS}，T_{DTS}=TDTS； DTS[7:5]=10x=>DT=（64+DTS[5:0])×T_{DTS}，T_{DTS}=2×T_{DTS}；

Field	Name	R/W	Description
			DTS[7:5]=110=>DT=（32+DTS[4:0])×T_{DTS}，T_{DTS}=8×T_{DTS}； DTS[7:5]=111=>DT=（32+DTS[4:0]）×T_{DTS}，T_{DTS}=16×T_{DTS}； For example: assuming T_{DTS} =125ns (8MHZ), the dead time setting is as follows: If the step time is 125ns, the dead time can be set from 0 to 15875ns; If the step time is 250ns, the dead time can be set from 16μs to 31750ns; If the step time is 1μs, the dead time can be set from 32μs to 63μs; If the step time is 2μs, the dead time can be set from 64μs to 126μs. Note: Once LOCK level (LOCKCFG bit in TMR1_BDT register) is set to 1, 2 or 3, these bits cannot be modified.
9:8	LOCKCFG	R/W	Lock Write Protection Mode Configure 00: Without Lock write protection level; the register can be written directly 01: Lock write protection level 1 It cannot be written to DTS, BRKEN, BRKPOL and AOEN bits of TMR1_BDT, and OCxOIS and OCxNOIS bits of TMR1_CTRL2 register. 10: Lock write protection level 2 It is not allowed to write to all bits with protection level 1 and write to the CCxPOL and OCxNPOL bits in TMR1_CCEN register and the RMOS and IMOS bits in TMR1_BDT register. 11: Lock write protection level 3 It is not allowed to write to all bits with protection level 2, and write to the OCxMOD and OCxPEN bits of TMR1_CCMx register. Note: After system reset, the lock write protect bit can only be written once.
10	IMOS	R/W	Idle Mode Off-state Configure Idle mode means MOEN=0; disable means CcxEN=0; this bit describes the impact of different values for this bit on the output waveform when MOEN=0 and CcxEN changes from 0 to 1. 0: OCx/OCxN output is disabled 1: If CCxEN=1, the invalid level is output during the dead time (the specific level value is affected by the polarity configuration), and the idle level is output after the dead time
11	RMOS	R/W	Run Mode Off-state Configure Run mode means MOEN=1; disable means CcxEN=0; this bit describes the impact of different values for this bit on the output waveform when MOEN=1 and CcxEN changes from 0 to 1. 0: OCx/OCxN output is disabled 1: OCx/OCxN first outptus invalid level (the specific level value is affected by the polarity configuration)
12	BRKEN	R/W	Break Function Enable 0: Disable 1: Enable Note: When the protection level is 1, this bit cannot be modified.
13	BRKPOL	R/W	Break Polarity Configure 0: The break input BRK is valid at low level 1: The break input BRK is valid at high level Note: When the protection level is 1, this bit cannot be modified. Writing to this bit requires an APB clock delay before it can be used.
14	AOEN	R/W	Automatic Output Enable 0: MOEN can only be set to 1 by software 1: MOEN can be set to 1 by software or be automatically set to 1 in next update event (breaking input is ineffective)

Field	Name	R/W	Description
			Note: When the protection level is 1, this bit cannot be modified.
15	MOEN	R/W	Wave Main Output Enable 0: Disable the output of OCx and OCxN or force the output of idle state 1: When CCxEN and CCxNEN bits of the TMR1_CCEN register are set, turn on OCx and OCxN output When the break input is valid, it is cleared by hardware asynchronously. Note: Setting to 1 by software or setting to 1 automatically depends on AOEN bit of the TMR1_BDT register.

13.6.19 DMA control register (TMR1_DCTRL)

Offset address: 0x48

Reset value: 0x0000

Field	Name	R/W	Description
4:0	DBADDR	R/W	DMA Base Address Setup These bits define the base address of DMA in continuous mode (when reading or writing TMR1_DMADDR register), and DBADDR is defined as the offset from the address of TMR1_CTRL1 register: 00000：TMR1_CTRL1 00001：TMR1_CTRL2 00010：TMR1_SMCTRL
7:5	Reserved		
12:8	DBLEN	R/W	DMA Burst Transfer Length Setup These bits define the transfer length and transfer times of DMA in continuous mode. The data transferred can be 16 bits and 8 bits. When reading/writing TMR1_DMADDR register, the timer will conduct a continuous transmission; 00000: Transmission for 1 time 00001: Transmission for 2 times 00010: Transmission for 3 times …… 10001: Transmission for 18 times The transmission address formula is as follows: Transmission address=TMR1_CTRL1 address (slave address) +DBADDR+DMA index; DMA index=DBLEN For example: DBLEN=7, DBADDR=TMR1_CTRL1 (slave address) means the address of the data to be transmitted, while the address +DBADDR+7 of TMR1_CTRL1 means the address of the data to be written/read Data transmission will occur to: TMR1_CTRL1 address + seven registers starting from DBADDR. The data transmission will change according to different DMA data length: (1) When the transmission data is set to 16 bits, the data will be transmitted to seven registers (2) When the transmission data is set to 8 bits, the data of the first register is the MSB bit of the first data, the data of the second register is the LSB bit of the first data, and the data will still be transmitted to seven registers.
15:13	Reserved		

13.6.20 DMA address register of continuous mode (TMR1_DMADDR)

Offset address: 0x4C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	DMADDR	R/W	DMA Register for Burst Transfer Read or write operation access of TMR1_DMADDR register may lead to access operation of the register in the following address: TMR1_CTRL1 address + (DBADDR+DMA index) ×4 Wherein: "TMR1_CTRL1 address" is the address of control register 1 (TMR1_CTRL1); "DBADDR" is the base address defined in TMR1_DCTRL register; "DMA index" is the offset automatically controlled by DMA, and it depends on DBLEN defined in TMR1_DCTRL register.

14 General-purpose Timer (TMR3)

14.1 Introduction

The general-purpose timer takes the time base unit as the core, and has the functions of input capture and output compare, and can be used to measure the pulse width, frequency and duty cycle, and generate the output waveform. It includes a 16-bit auto reload counter (realize count-up, count-down and center-aligned count).

The timer and timer are independent of each other, and they can achieve synchronization and cascading.

14.2 Main Characteristics

（1） Timebase unit
- Counter: 16-bit counter, count-up, count-down and center-aligned count
- Prescaler: 16-bit programmable prescaler
- Auto reloading function

（2） Clock source selection
- Internal clock
- External input
- External trigger
- Internal trigger

（3） Input function
- Counting function
- PWM input
- Encoder interface mode

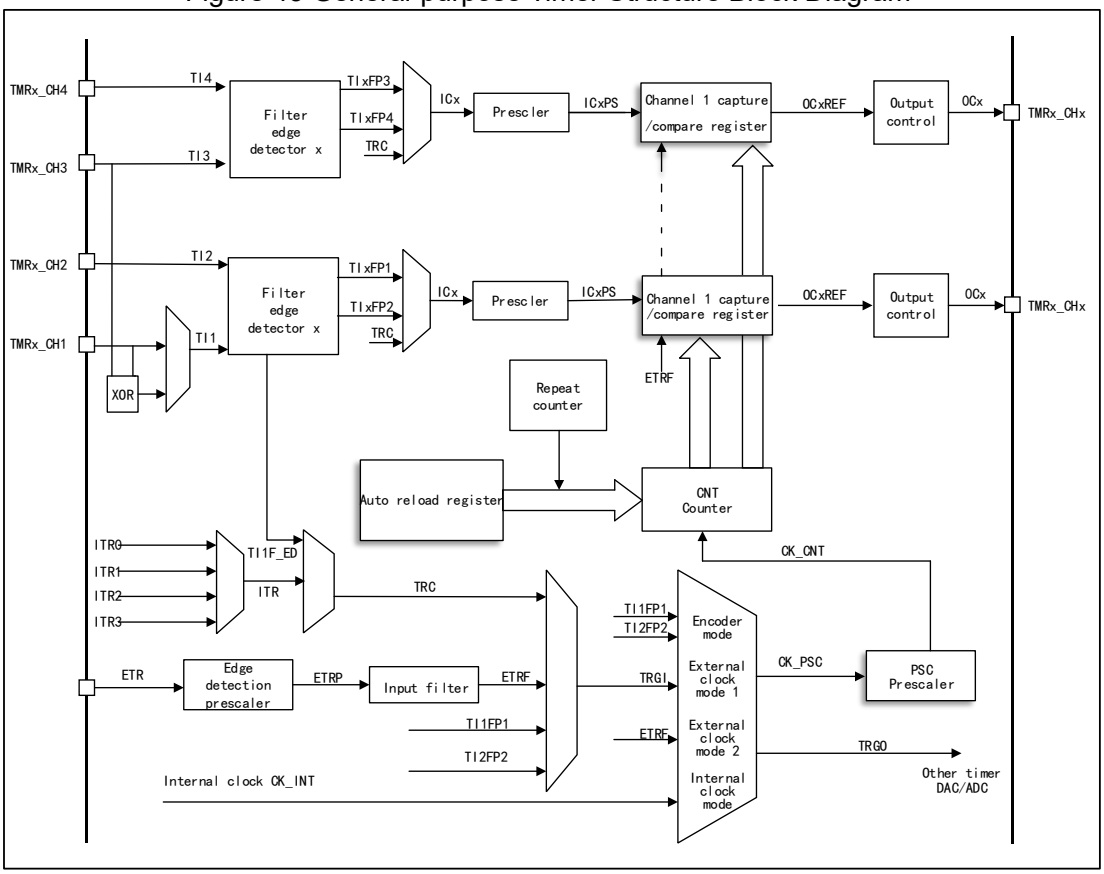
（4） Output function
- PWM output mode
- Forced output mode
- Single-pulse mode

（5） Master/Slave mode controller of timer
- Timers can be synchronized and cascaded
- Support multiple slave modes and synchronization signals

（6） Interrupt and DMA request event
- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Input capture
- Output compare

14.3 Structure Block Diagram

Figure 43 General-purpose Timer Structure Block Diagram



14.4 Functional Description

14.4.1 Clock Source Selection

The general-purpose timer has four clock sources

Internal clock

It is TMR3_CLK from RCM, namely the driving clock of the timer; when the slave mode controller is disabled, the clock source CK_PSC of the prescaler is driven by the internal clock CK_INT.

External clock mode 1

The trigger signal generated from the input channel TI1/2/3/4 of the timer after polarity selection and filtering is connected to the slave mode controller to control the work of the counter. Besides, the pulse signal generated by the input of Channel 1 after double-edge detection of the rising edge and the falling edge is logically equal or the future signal is TI1F_ED signal, namely double-edge signal of TIF_ED. Specially the PWM input can only be input by TI1/2.

External clock mode 2

After polarity selection, frequency division and filtering, the signal from external trigger interface (ETR) is connected to slave mode controller through trigger input selector to control the work of counter.

Internal trigger input

The timer is set to work in slave mode, and the clock source is the output signal of other timers. At this time, the clock source has no filtering, and the synchronization or cascading between timers can be realized. The master mode timer can reset, start, stop or provide clock for the slave mode timer.

14.4.2 Timebase Unit

The time base unit in the general-purpose timer contains three registers

- Counter register (CNT) 16 bits
- Auto reload register (AUTORLD) 16 bits
- Prescaler register (PSC) 16 bits

Counter CNT

There are three counting modes for the counter in the general-purpose timer

- Count-up mode
- Count-down mode
- Center-aligned mode

Count-up mode

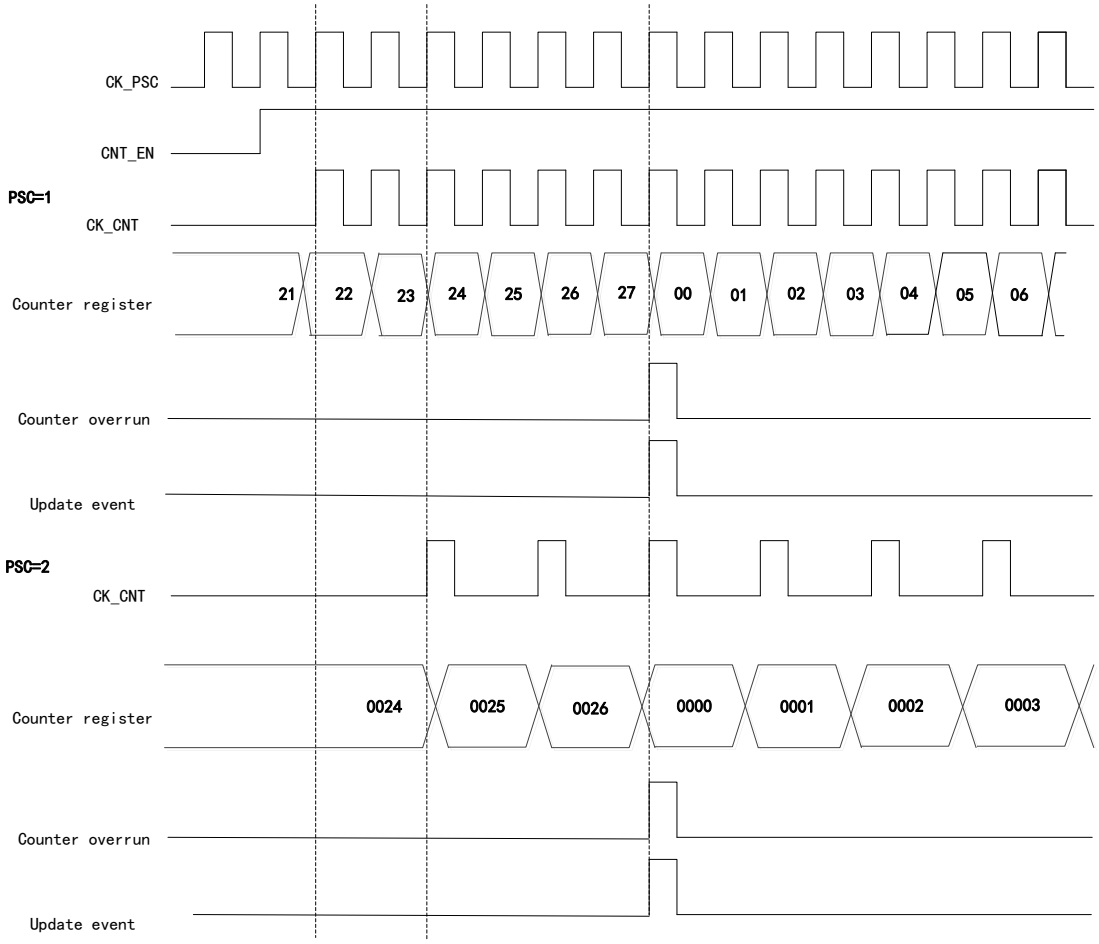
Set to the count-up mode by CNTDIR bit of configuration control register (TMR3_CTRL1).

When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMR3_CNT) is equal to the value of the auto reload (TMR3_AUTORLD), the counter will start to count again from 0, a count-up overrun event will be generated, and the value of the auto reload (TMR3_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by UD bit of configuration control register TMR3_CTRL1.

The figure below is Timing Diagram when Division Factor is 1 or 2 in Count-up Mode

Figure 44 Timing Diagram when Division Factor is 1 or 2 in Count-up Mode



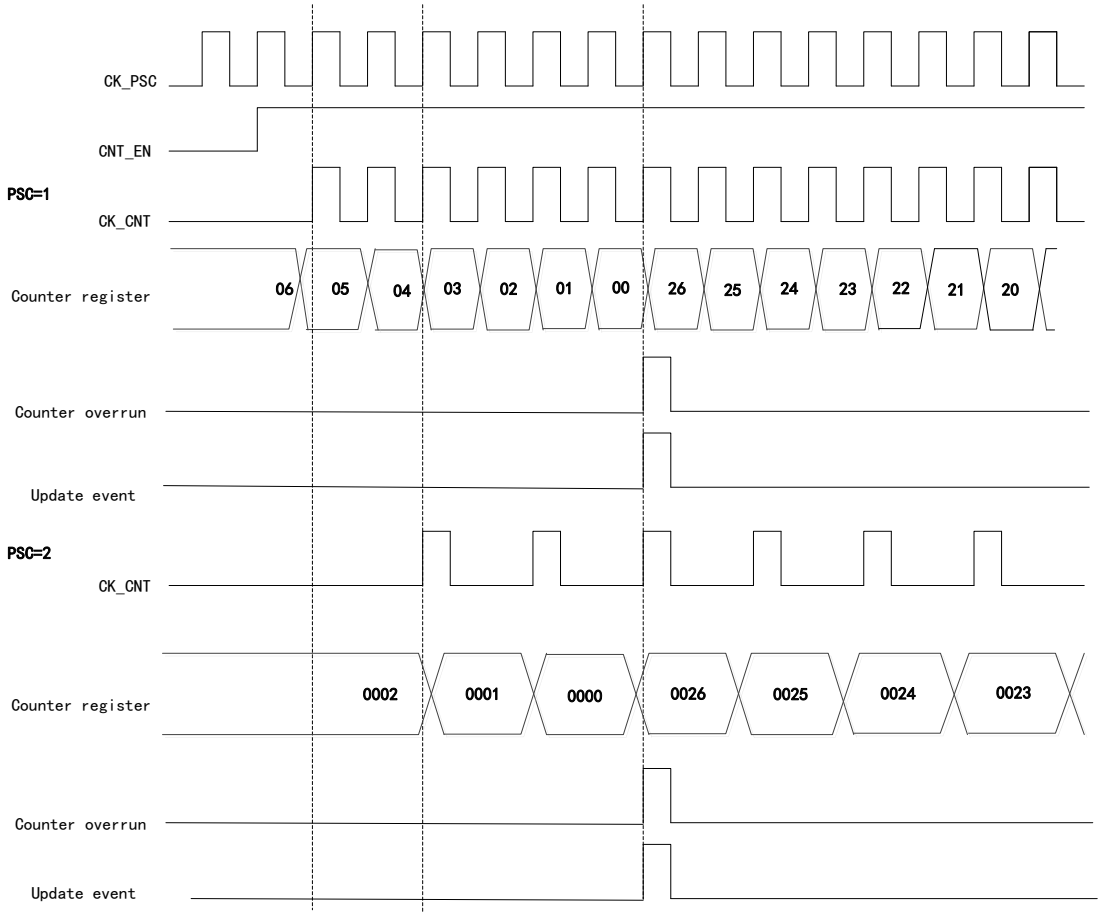
Count-down mode

Set to the count-down mode by CNTDIR bit of configuration control register (TMR3_CTRL1).

When the counter is in count-down mode, the counter will start to count down from the value of the auto reload (TMR3_AUTORLD); every time a pulse is generated, the counter will decrease by 1 and when it becomes 0, the counter will start to count again from (TMR3_AUTORLD), meanwhile, a count-down overrun event will be generated, and the value of the auto reload (TMR3_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by configuring the UD bit of the TMR3_CTRL1 register.

Figure 45 Timing Diagram when Division Factor is 1 or 2 in Count-down Mode

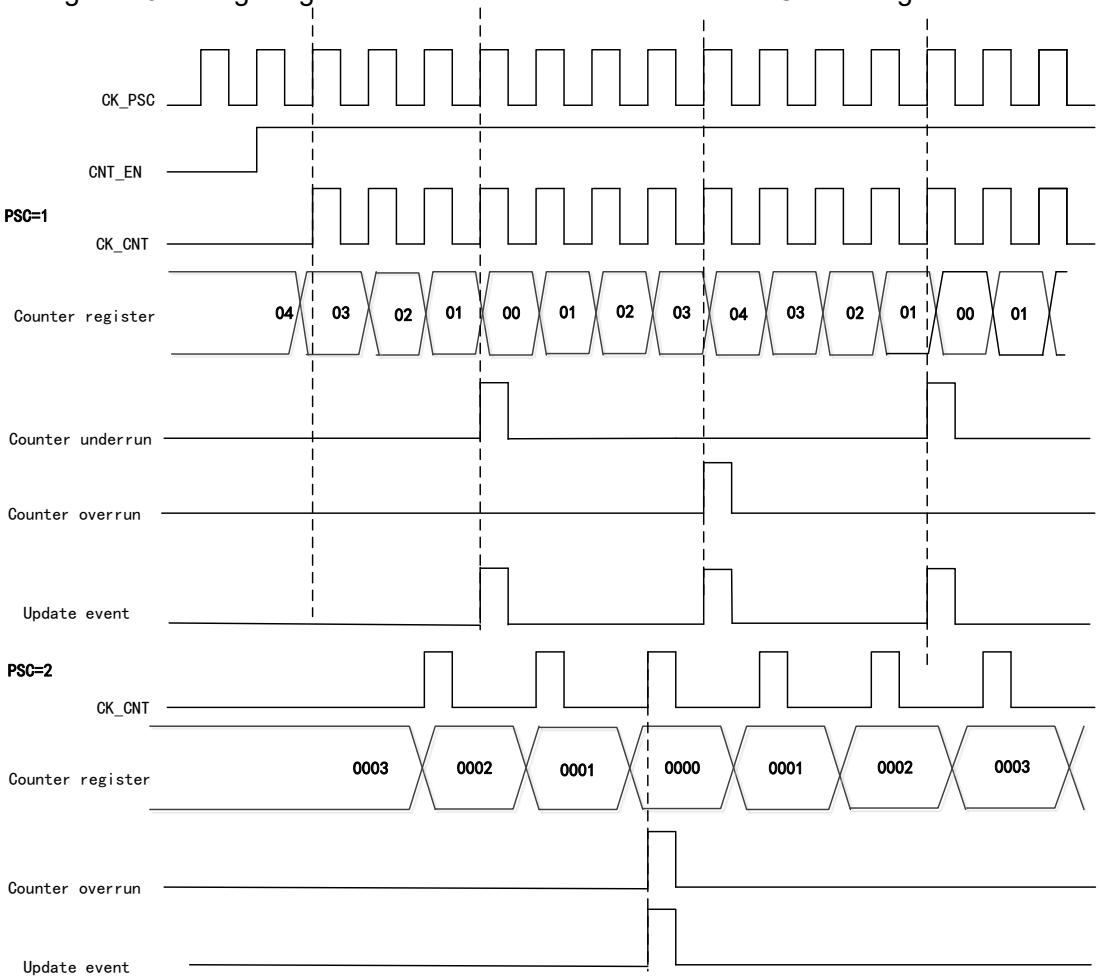


Center-aligned mode

Set to the center-aligned mode by CNTDIR bit of configuration control register (TMR3_CTRL1).

When the counter is in center-aligned mode, the counter counts up from 0 to the value of auto reload (TMR3_AUTORLD), then counts down to 0 from the value of the auto reload (TMR3_AUTORLD), which will repeat; in counting up, when the counter value is (AUTORLD-1), a counter overrun event will be generated; in counting down, when the counter value is 1, a counter underrun event will be generated.

Figure 46 Timing Diagram when Division Factor is 1 or 2 in Center-aligned Mode



Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value between 1 and 65536 (controlled by TMR3_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

14.4.3 Input Capture

Input capture channel

The general-purpose timer has four independent capture/compare channels, each of which is surrounded by a capture/compare register.

In the input capture, the measured signal will enter from the external pin T1/2/3/4 of the timer, first pass through the edge detector and input filter, and then into the capture channel. Each capture channel has a corresponding capture register. When the capture occurs, the value of the counter CNT will be latched in the capture register CCx. Before entering the capture register, the signal will pass through the prescaler, which is used to set how many events to capture at a time.

Input capture application

Input capture is used to capture external events, and can give the time flag to indicate the occurrence time of the event and measure the pulse jump edge events (measure the frequency or pulse width), for example, if the selected edge appears on the input pin, the TMR3_CCx register will capture the current value of the counter and the CCxIFLG bit of the state register TMR3_STS will be set to 1; if CCxIEN=1, an interrupt will be generated.

In capture mode, the timing, frequency, period and duty cycle of a waveform can be measured. In the input capture mode, the edge selection is set to rising edge detection. When the rising edge appears on the capture channel, the first capture occurs, at this time, the value of the counter CNT will be latched in the capture register CCx; at the same time, it will enter the capture interrupt, a capture will be recorded in the interrupt service program and the value will be recorded. When the next rising edge is detected, the second capture occurs, the value of counter CNT will be latched in capture register CCx again, at this time, it will enter the capture interrupt again, the value of capture register will be read, and the cycle of this pulse signal will be obtained through capture.

14.4.4 Output Compare

There are eight modes of output compare: freeze, channel x is valid level when matching, channel x is invalid level when matching, flip, force is invalid, force is valid, PWM1 and PWM2 modes, which are configured by OCxMOD bit in TMR3_CCMx register and can control the waveform of output signal in output compare mode.

Output compare application

In the output compare mode, the position, polarity, frequency and time of the pulse generated by the timer can be controlled.

When the value of the counter is equal to that of the capture/compare register, the channel output can be set as high level, low level or flip by configuring the OCxMOD bit in TMR3_CCMx register and the CCxPOL bit in the output polarity TMR3_CCEN register.

When CCxIFLG=1 in TMR3_STS register, if CCxIEN=1 in TMR3_DIEN register, an interrupt will be generated; if CCDSEL=1 in TMR3_CTRL2 register, DMA request will be generated.

14.4.5 PWM Output Mode

PWM mode is an adjustable pulse signal output by the timer. The pulse width of the signal is determined by the value of the compare register CCx, and the cycle is determined by the value of the auto reload AUTORLD.

PWM output mode contains PWM mode 1 and PWM mode 2; PWM mode 1 and PWM mode 2 are divided into count-up, count-down and edge alignment counting; in PWM mode 1, if the value of the counter CNT is less than the value of the compare register CCx, the output level will be valid; otherwise, it will be invalid.

Set the timing diagram in PWM mode 1 when CCx=5, AUTORLD=7

Figure 47 PWM1 Count-up Mode Timing Diagram

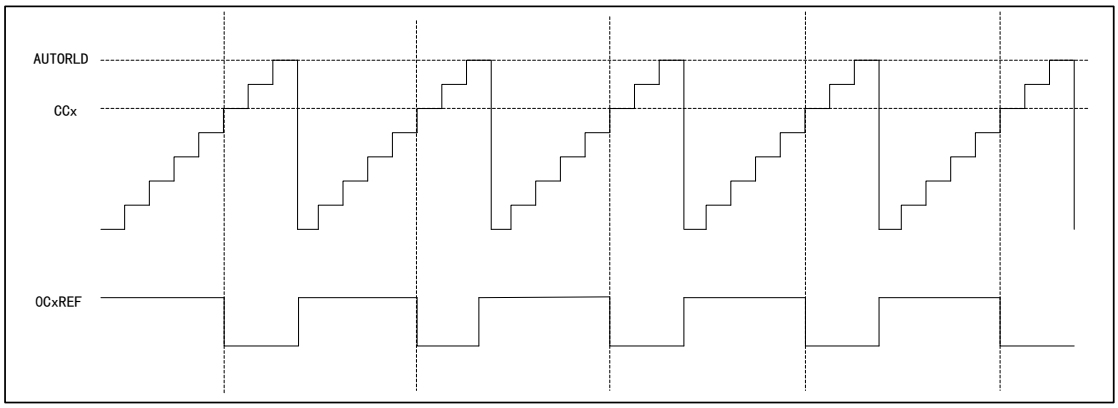


Figure 48 PWM1 Count-down Mode Timing Diagram

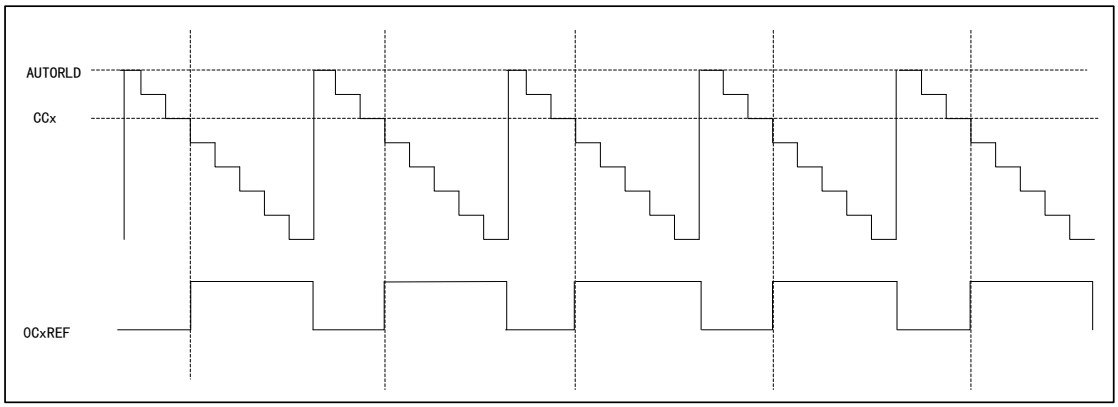
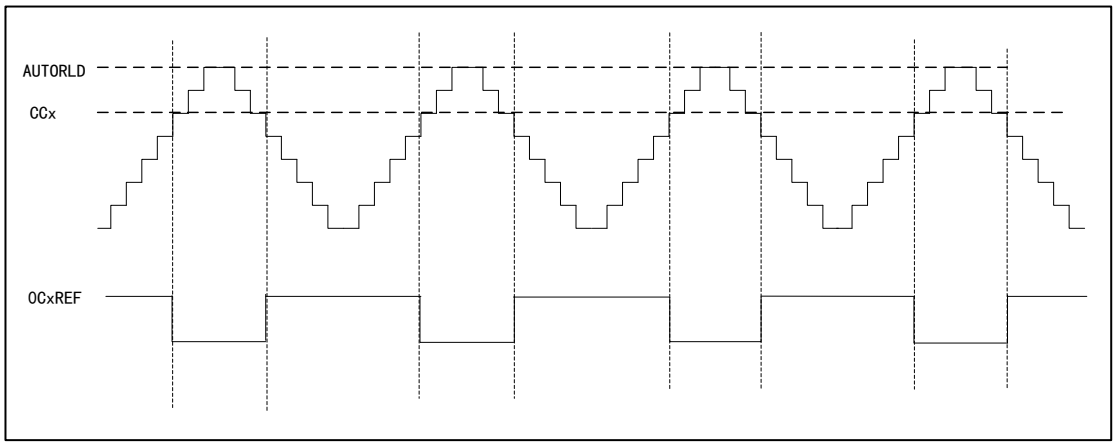


Figure 49 PWM1 Center-aligned Mode Timing Diagram



In PWM mode 2, if the value of the counter CNT is less than that of the compare register CCx, the output level will be invalid; otherwise, it will be valid.

Set the timing diagram in PWM mode 2 when CCx=5, AUTORLD=7

Figure 50 PWM2 Count-up Mode Timing Diagram

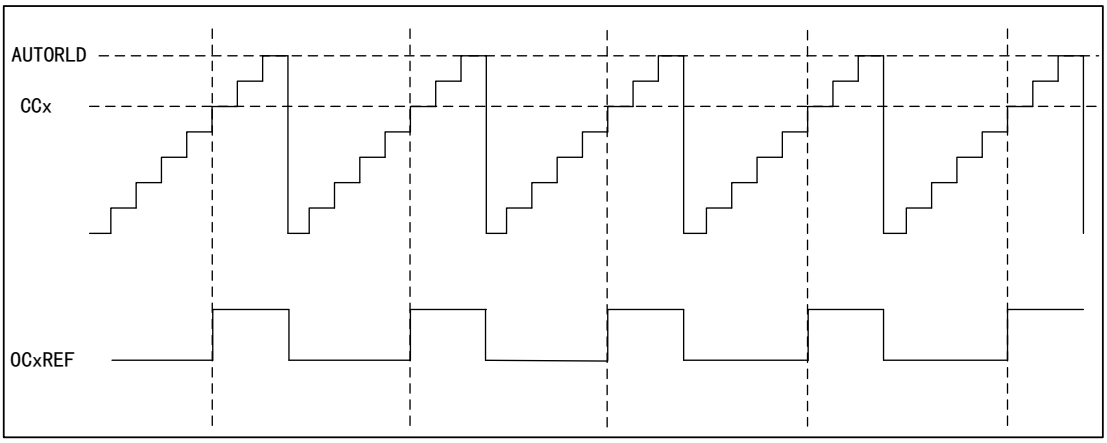


Figure 51 PWM2 Count-down Mode Timing Diagram

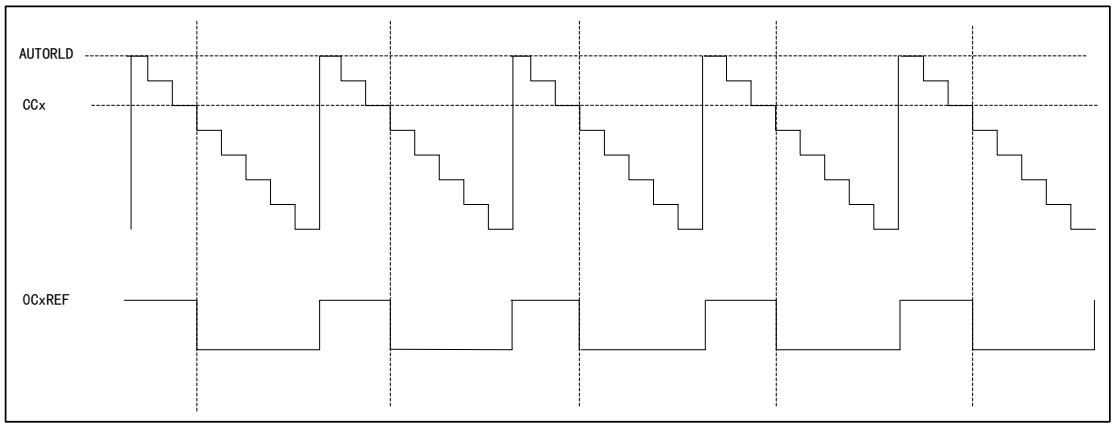
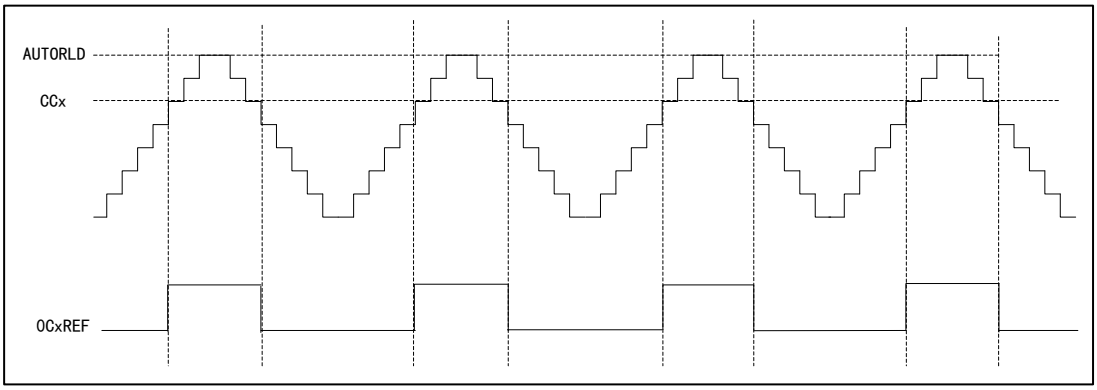


Figure 52 PWM2 Center-aligned Mode Timing Diagram



14.4.6 PWM Input Mode

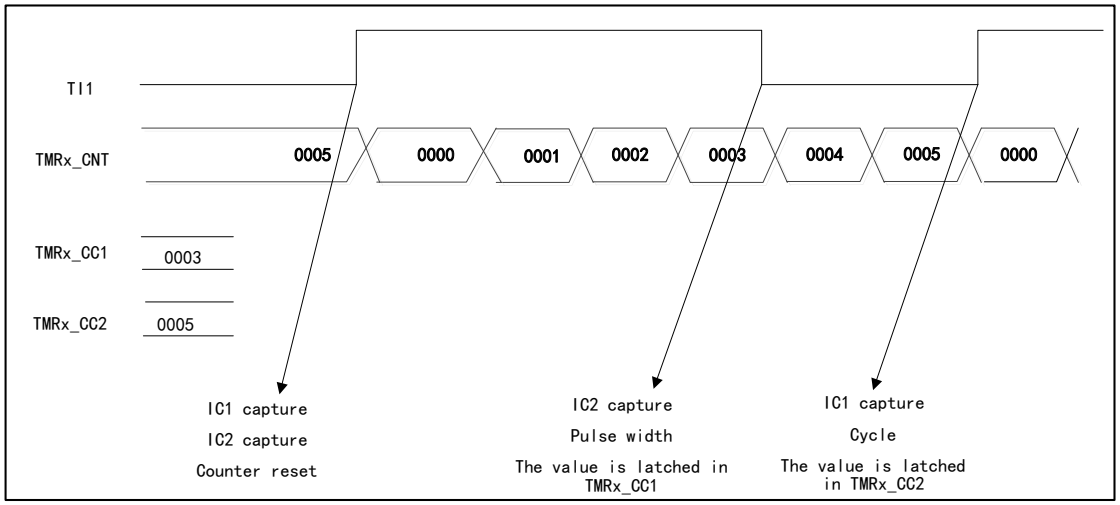
PWM input mode is a particular case of input capture.

In PWM input mode, as only TI1FP1 and TI1FP2 are connected to the slave mode controller, input can be performed only through the channels TMR3_CH1 and TMR3_CH2, which need to occupy the capture registers of CH1 and CH2.

In the PWM input mode, the PWM signal enters from TMR3_CH1, and the signal will be divided into two channels, one can measure the cycle and the other can measure the duty cycle. In the configuration, it is only required to set the polarity of one channel, and the other will be automatically configured with the opposite polarity.

In this mode, the slave mode controller should be configured as the reset mode (SMFSEL bit of TMR3_SMCTRL register)

Figure 53 Timing Diagram in PWM Input Mode



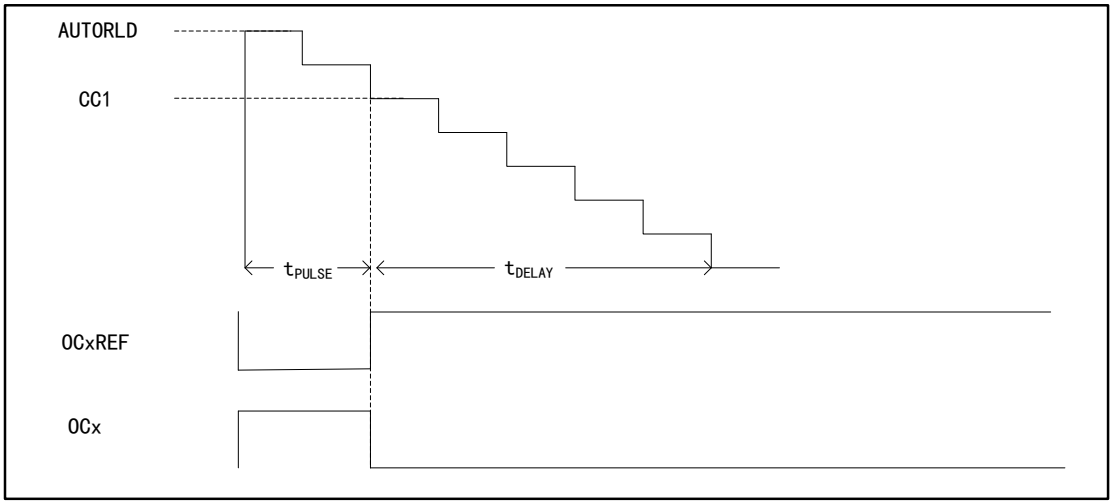
14.4.7 Single-pulse Mode

The single-pulse mode is a special case of timer compare output, and is also a special case of PWM output mode.

Set SPMEN bit of TMR3_CTRL1 register, and select the single-pulse mode. After the counter is started, a certain number of pulses will be output before the update event occurs. When an update event occurs, the counter will stop counting, and the subsequent PWM waveform output will no longer be changed.

After a certain controllable delay, a pulse with controllable pulse width is generated in single-pulse mode through the program. The delay time is defined by the value of TMR3_CCx register; in the count-up mode, the delay time is CCx and the pulse width is AUTORLD-CCx; in the count-down mode, the delay time is AUTORLD-CCx and the pulse width is CCx.

Figure 54 Timing Diagram in Single-pulse Mode



14.4.8 Forced Output Mode

In the forced output mode, the compare result is ignored, and the corresponding level is directly output according to the configuration instruction.

- CCxSEL=00 for TMR3_CCMx register, set CCx channel as output
- OCxMOD=100/101 for TMR3_CCMx register, set to force OCxREF signal to invalid/valid state

In this mode, the corresponding interrupt and DMA request will still be generated.

14.4.9 Encoder Interface Mode

The encoder interface mode is equivalent to an external clock with direction selection. In the encoder interface mode, the content of the timer can always indicate the position of the encoder.

The selection methods of encoder interface is as follows:

- By setting SMFSEL bit of TMR3_SMCTRL register, set the counter to count on the edge of TI1 channel /TI2 channel, or count on the edge of TI1 and TI2 at the same time.
- Select the polarity of TI1 and TI2 by setting the CC1POL and CC2POL bits of TMR3_CCEN register.
- Select to filter or not by setting the IC1F and IC2F bits of TMR3_CCM1 register.

The two input TI1 and TI2 can be used as the interface of incremental encoder. The counter is driven by the effective jump of the signals TI1FP1 and TI2FP2 after filtering and edge selection in TI1 and TI2.

The count pulse and direction signal are generated according to the input signals of TI1 and TI2

- The counter will count up/down according to the jumping sequence of the input signal
- Set CNTDIR of control register TMR3_CTRL1 to be read-only (CNTDIR will be re-calculated due to jumping of any input end)

The change mechanism of counter count direction is shown in the figure below

Table 45 Relationship between Count Direction and Encoder

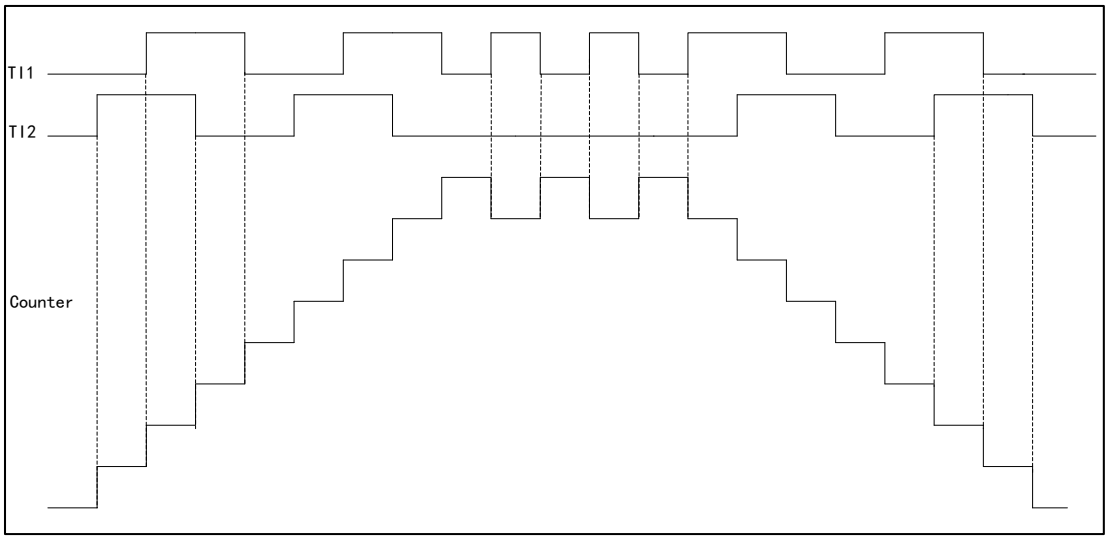
Effective edge		Count only in TI1		Count only in TI2		Count in both TI1 and TI2	
Level of relative signal		High	Low	High	Low	High	Low
TI1FP1	Rising edge	Count down	Count up	—		Count down	Count up
	Falling edge	Count up	Count down			Count up	Count down
TI2FP2	Rising edge	—		Count up	Count down	Count up	Count down
	Falling edge			Count down	Count up	Count down	Count up

The external incremental encoder can be directly connected with MCU, not needing external interface logic, so the comparator is used to convert the differential output of the encoder to digital signal to increase the immunity from noise interference.

Among the following examples,

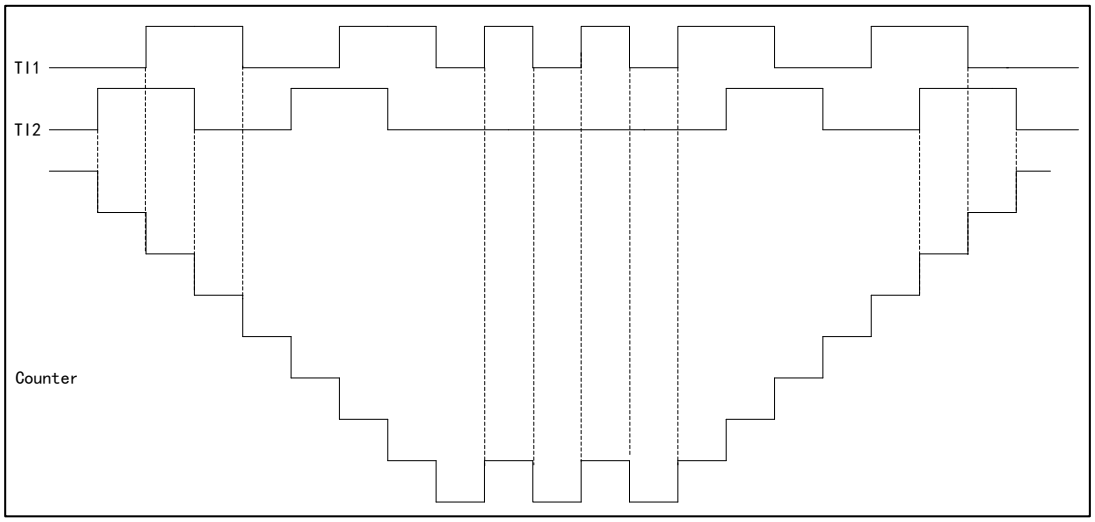
- TI1FP1 is mapped to TI1
- TI2FP2 is mapped to TI2
- Neither TI1FP1 nor TI2FP2 is reverse phase
- The input signal is valid at the rising edge and falling edge
- Enable the counter

Figure 55 Counter Operation Example in Encoder Mode



For example, when TI1 is at low level, and TI2 is in rising edge state, the counter will count up.

Figure 56 Example of Encoder Interface Mode of TI1FP1 Reversed Phase



For example, when TI1 is at low level, and the rising edge of TI2 jumps, the counter will count down.

14.4.10 Slave Mode

TMR3 timer can synchronize external trigger

- Reset mode
- Gated mode
- Trigger mode

SMFSEL bit in TMR3_SMCTRL register can be set to select the mode

SMFSEL=100 set the reset mode, SMFSEL=101 set the gated mode, SMFSEL=110 set the trigger mode.

In the reset mode, when a trigger input event occurs, the counter and prescaler will be initialized, and the rising edge of the selected trigger input (TRGI) will reinitialize the counter and generate a signal to update the register.

In the gated mode, the enable of the counter depends on the high level of the selected input. When the trigger input is high, the clock of the counter will be started. Once the trigger input becomes low, the counter will stop (but not be reset). The start and stop of the counter are controlled.

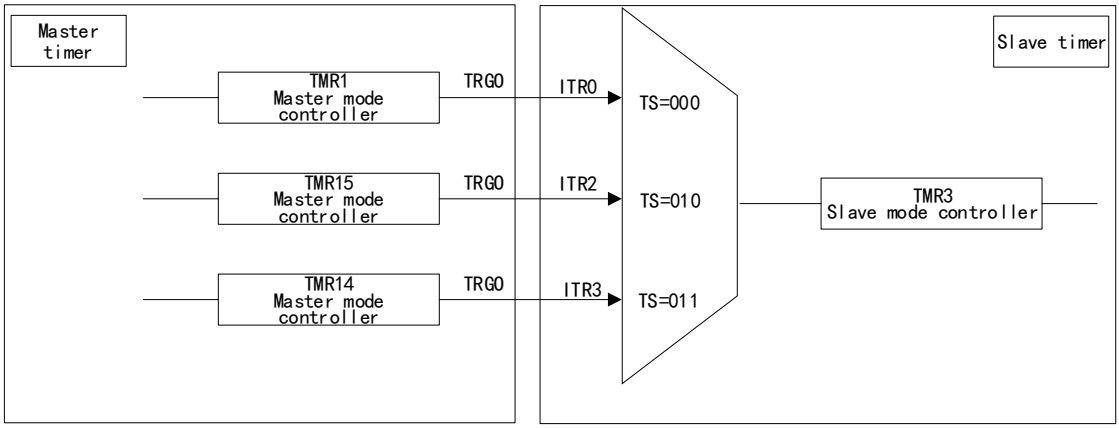
In the trigger mode, the enable of the counter depends on the event on the selected input, the counter is started (but is not reset) at the rising edge of the trigger input, and only the start of the counter is controlled.

14.4.11 Timer Interconnection

Each timer of TMRx can realize synchronization or cascading between timers. It is required to configure one timer in master mode and the other timer in slave mode.

When the timer is in master mode, it can reset, start, stop and provide clock source for the counter of the slave mode timer.

Figure 57 Interconnection of TMR3 and Other Timers



Note: The trigger signal for the TMR14 internal connection is TMR14_CH1.

When the timers are interconnected:

- A timer can be used as the prescaler of other register
- Another register can be started by the enable signal of a timer
- Another register can be started by the update event of a timer
- Another register can be selected by the enable of a timer
- Two timers can be synchronized by an external trigger

14.4.12 Interrupt and DMA Request

The timer can generate an interrupt when an event occurs during operation

- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Compare event

Some internal interrupt events can generate DMA requests, and special interfaces can enable or disable DMA requests.

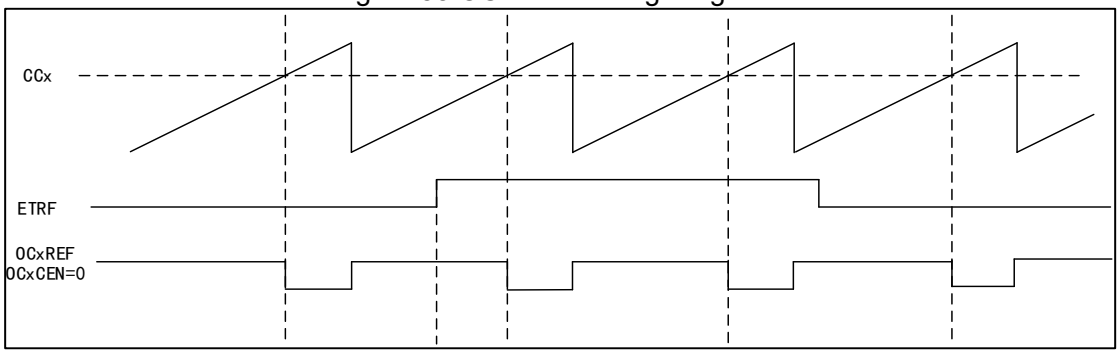
14.4.13 Clear OCxREF signal when external events occur

This function is used for output compare and PWM mode.

In one channel, the high level of ETRF input port will reduce the signal of OCxREF to low level, and the OCxCEN bit in capture/compare register TMR3_CCMx is set to 1, and OCxREF signal will remain low until the next update event.

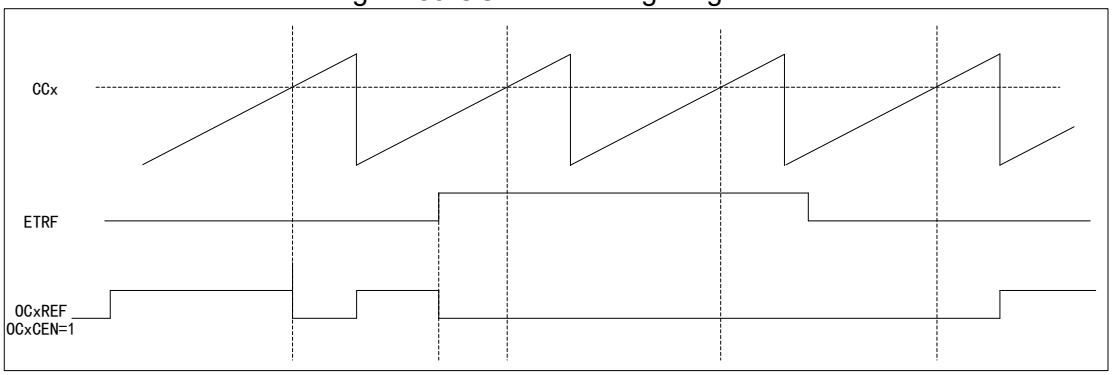
Set TMR3 to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=0, and the output OCxREF signal is shown in the figure below.

Figure 58 OCxREF Timing Diagram



Set TMR3 to PWM mode, close the external trigger prescaler, and disable the external trigger mode 2; when ETRF input is high, set OCxCEN=1, and the output OCxREF signal is shown in the figure below.

Figure 59 OCxREF Timing Diagram



14.5 Register Address Mapping

In the following table, all registers of TMR3 are mapped to a 16-bit addressable (address) space.

Table 46 TMR3 Register Mapping

Register name	Description	Offset address
TMR3_CTRL1	Control register 1	0x00
TMR3_CTRL2	Control register 2	0x04
TMR3_SMCTRL	Slave mode control register	0x08
TMR3_DIEN	DMA/Interrupt enable register	0x0C
TMR3_STS	State register	0x10
TMR3_CEG	Control event generation register	0x14
TMR3_CCM1	Capture/Compare mode register 1	0x18
TMR3_CCM2	Capture/Compare mode register 2	0x1C
TMR3_CCEN	Capture/Compare enable register	0x20
TMR3_CNT	Counter register	0x24
TMR3_PSC	Prescaler register	0x28

Register name	Description	Offset address
TMR3_AUTORLD	Auto reload register	0x2C
TMR3_CC1	Channel 1 capture/compare register	0x34
TMR3_CC2	Channel 2 capture/compare register	0x38
TMR3_CC3	Channel 3 capture/compare register	0x3C
TMR3_CC4	Channel 4 capture/compare register	0x40
TMR3_DCTRL	DMA control register	0x48
TMR3_DMADDR	DMA address register of continuous mode	0x4C

14.6 Register Functional Description

14.6.1 Control register 1 (TMR3_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.
1	UD	R/W	Update Disable Update event can cause AUTORLD, PSC and CCx to generate the value of update setting. 0: Update event is allowed (UEV) An update event can occur in any of the following situations: The counter overruns/underruns; Set UEG bit; Update generated by slave mode controller. 1: Update event is disabled
2	URSSEL	R/W	Update Request Source Select If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit. 0: The counter overruns or underruns Set UEG bit Update generated by slave mode controller 1: The counter overruns or underruns
3	SPMEN	R/W	ingle Pulse Mode Enable When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed. 0: Disable 1: Enable
4	CNTDIR	R/W	Counter Direction This bit is read-only when the counter is configured as center-aligned mode or encoder mode. 0: Count up

Field	Name	R/W	Description
			1: Count down
6:5	CAMSEL	R/W	Center Aligned Mode Select) In the center-aligned mode, the counter counts up and down alternately; otherwise, it will only count up or down. Different center-aligned modes affect the timing of setting the output compare interrupt flag bit of the output channel to 1; when the counter is disabled (CNTEN=0), select the center-aligned mode. 00: Edge alignment mode 01: Center-aligned mode 1 (the output compare interrupt flag bit of output channel is set to 1 when counting down) 10: Center-aligned mode 2 (the output compare interrupt flag bit of output channel is set to 1 when counting up) 11: Center-aligned mode 3 (the output compare interrupt flag bit of output channel is set to 1 when counting up/down)
7	ARPEN	R/W	Auto-reload Preload Enable When the buffer is disabled, the program modification TMR3_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMR3_AUTORLD will modify the values loaded to the counter in the next update event. 0: Disable 1: Enable
9:8	CLKDIV	R/W	Clock Divide Factor For the configuration of dead time and digital filter, CK_INT provides the clock, and the dead time and the clock of the digital filter can be adjusted by setting this bit. 00：$t_{DTS}=t_{CK\_INT}$ 01：$t_{DTS}=2\times t_{CK\_INT}$ 10：$t_{DTS}=4\times t_{CK\_INT}$ 11: Reserved
15:10	Reserved		

14.6.2 Control register 2 (TMR3_CTRL2)

Offset address: 0x04

Reset value: 0x0000

Field	Name	R/W	Description
2:0	Reserved		
3	CCDSEL	R/W	Capture/compare DMA Select 0: Send DMA request of CCx when CCx event occurs 1: Send DMA request of CCx when an update event occurs
6:4	MMSEL	R/W	Master Mode Signal Select The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with master timer, and specifically affects the configuration of timers in slave mode. 000: Reset; the reset signal of master mode timer is used for TRGO 001: Enable; the counter enable signal of master mode timer is used for TRGO 010: Update; the update event of master mode timer is used for TRGO 011: Compare pulses; when the master mode timer captures/compares successfully (CCxIFLG=1), a pulse signal is output for TRGO

Field	Name	R/W	Description
			100: Comparison mode 1; OC1REF is used to trigger TRGO 101: Comparison mode 2; OC2REF is used to trigger TRGO 110: Comparison mode 3; OC3REF is used to trigger TRGO 111: Comparison mode 4; OC4REF is used to trigger TRGO
7	TI1SEL	R/W	Timer Input 1 Select 0: TMR3_CH1 pin is connected to TI1 input 1: TMR3_CH1, TMR3_CH2 and TMR3_CH3 pins are connected to TI1 input after exclusive
15:8	Reserved		

14.6.3 Slave mode control register (TMR3_SMCTRL)

Offset address: 0x08

Reset value: 0x0000

Field	Name	R/W	Description
2:0	SMFSEL	R/W	Slave Mode Function Select 000: Disable the slave mode, the timer can be used as master mode timer to affect the work of slave mode timer; if CTRL1_CNTEN=1, the prescaler is directly driven by the internal clock. 001: Encoder mode 1; according to the level of TI1FP1, the counter counts at the edge of TI2FP2. 010: Encoder mode 2; according to the level of TI2FP2, the counter counts at the edge of TI1FP1. 011: Encoder mode 3; according to the input level of another signal, the counter counts at the edge of TI1FP1 and TI2FP2. 100: Reset mode; the slave mode timer resets the counter after receiving the rising edge signal of TRGI and generates the signal to update the register. 101: Gated mode; the slave mode timer starts the counter to work after receiving the TRGI high level signal; it stops the counter when receiving TRGI low level; when receiving TRGI high level signal again, the timer will continue to work; the counter is not reset during the whole period. 110: Trigger mode, the slave mode timer starts the counter to work after receiving the rising edge signal of TRGI. 111: External clock mode 1; select the rising edge signal of TRGI as the clock source to drive the counter to work.
3	OCCSEL	R/W	OCREF Clear Source Select This bit is used to select OCREF clear source 0：OCREF_CLR 1：ETRF
6:4	TRGSEL	R/W	Select the trigger input signal (Trigger Input Signal Select) In order to avoid false edge detection when changing the bit value, it must be changed when SMFSEL=0. 000: Internal trigger ITR0 001: Reserved 010: Internal trigger ITR2 011: Reserved 100: Channel 1 input edge detector TIF_ED 101: Channel 1 post-filtering timer input TI1FP1 110: Channel 2 post-filtering timer input TI2FP2 111: External trigger input (ETRF)

Field	Name	R/W	Description
7	MSMEN	R/W	Master/slave Mode Enable 0: Invalid 1: Enable the master/slave mode
11:8	ETFCFG	R/W	External Trigger Filter Configure 0000: Filter disabled, sampling by f_{DTS} 0001：DIV=1，N=2 0010：DIV=1，N=4 0011：DIV=1，N=8 0100：DIV=2，N=6 0101：DIV=2，N=8 0110：DIV=4，N=6 0111：DIV=4，N=8 1000：DIV=8，N=6 1001：DIV=8，N=8 1010：DIV=16，N=5 1011：DIV=16，N=6 1100：DIV=16，N=8 1101：DIV=32，N=5 1110：DIV=32，N=6 1111：DIV=32，N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, and a jump is generated by every N events.
13:12	ETPCFG	R/W	External Trigger Prescaler Configure The ETR (external trigger input) signal becomes ETRP after frequency division. The signal frequency of ETRP is at most 1/4 of TMR3CLK frequency; when ETR frequency is too high, the ETRP frequency must be reduced through frequency division. 00: The prescaler is disabled; 01: ETR signal 2 divided frequency 10: ETR signal 4 divided frequency 11: ETR signal 8 divided frequency
14	ECEN	R/W	External Clock Enable Mode2 0: Disable 1: Enable Setting ECEN bit has the same function as selecting external clock mode 1 to connect TRGI to ETRF; slave mode (reset, gating, trigger) can be used at the same time with external clock mode 2, but TRGI cannot be connected to ETRF in such case; when external clock mode 1 and external clock mode 2 are enabled at the same time, the input of external clock is ETRF.
15	ETPOL	R/W	External Trigger Polarity Configure This bit decides whether the external trigger ETR is reversed. 0: The external trigger ETR is not reversed,and the high level or rising edge is valid 1: The external trigger ETR is reversed, and the low level or falling edge is valid

Table 47 TMR3 Internal Trigger Connection

Slave timer	ITR0（TS=000）	ITR2（TS=010）
TMR3	TMR1	TMR15

14.6.4 DMA/Interrupt enable register (TMR3_DIEN)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
0	UIEN	R/W	Update interrupt Enable 0: Disable 1: Enable
1	CC1IEN	R/W	Capture/Compare Channel1 Interrupt Enable 0: Disable 1: Enable
2	CC2IEN	R/W	Capture/Compare Channel2 Interrupt Enable 0: Disable 1: Enable
3	CC3IEN	R/W	Capture/Compare Channel3 Interrupt Enable 0: Disable 1: Enable
4	CC4IEN	R/W	Capture/Compare Channel4 Interrupt Enable 0: Disable 1: Enable
5	Reserved		
6	TRGIEN	R/W	Trigger interrupt Enable 0: Disable 1: Enable
7	Reserved		
8	UDIEN	R/W	Update DMA Request Enable 0: Disable 1: Enable
9	CC1DEN	R/W	Capture/Compare Channel1 DMA Request Enable 0: Disable 1: Enable
10	CC2DEN	R/W	Capture/Compare Channel2 DMA Request Enable 0: Disable 1: Enable
11	CC3DEN	R/W	Capture/Compare Channel3 DMA Request Enable 0: Disable 1: Enable
12	CC4DEN	R/W	Capture/Compare Channel4 DMA Request Enable 0: Disable 1: Enable
13	Reserved		
14	TRGDEN	R/W	Trigger DMA Request Enable 0: Disable 1: Enable
15	Reserved		

14.6.5 State register (TMR3_STS)

Offset address: 0x10

Reset value: 0x0000

Field	Name	R/W	Description
0	UIFLG	RC_W0	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur

Field	Name	R/W	Description
			1: Update event interrupt occurs When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations: (1) UD=0 on TMR3_CTRL1 register, when overruns/underruns, an update event will be generated; (2) URSSEL=0 and UD=0 on TMR3_CTRL1 register, configure UEG=1 on TMR3_CEG register to generate update event, and the counter needs to be initialized by software; (3) URSSEL=0 and UD=0 on TMR3_CTRL1 register, generate update event when the counter is initialized by trigger event.
1	CC1IFLG	RC_W0	Capture/Compare Channel1 Interrupt Flag **When the capture/compare channel 1 is configured as output:** 0: No matching occurred 1: The value of TMR3_CNT matches the value of TMR3_CC1 **When the capture/compare channel 1 is configured as input:** 0: Input capture did not occur 1: Input capture occurred When a capture event occurs, the bit is set to 1 by hardware, and it can be cleared by software or cleared when reading TMR3_CC1 register.
2	CC2IFLG	RC_W0	Capture/Compare Channel2 i Interrupt Flag Refer to the description of CC1IFLG
3	CC3IFLG	RC_W0	Capture/Compare Channel3 Interrupt Flag Refer to the description of CC1IFLG
4	CC4IFLG	RC_W0	Captuer/Compare Channel4 Interrupt Flag Refer to the description of CC1IFLG
5	Reserved		
6	TRGIFLG	RC_W0	Trigger Event Interrupt Generate Flag 0: Trigger event interrupt did not occur 1: Trigger event interrupt occurred After Trigger event is generated, this bit is set to 1 by hardware and cleared by software.
8:7	Reserved		
9	CC1RCFLG	RC_W0	Capture/compare Channel1 Repetition Capture Flag 0: Repeat capture does not occur 1: Repeat capture occurs The value of the counter is captured to TMR3_CC1 register, and CC1IFLG=1; this bit is set to 1 by hardware and cleared by software only when the channel is configured as input capture.
10	CC2RCFLG	RC_W0	Capture/compare Channel2 Repetition Capture Flag Refer to the description of CC1RCFLG
11	CC3RCFLG	RC_W0	Capture/compare Channel3 Repetition Capture Flag Refer to the description of CC1RCFLG

Field	Name	R/W	Description
12	CC4RCFLG	RC_W0	Capture/compare Channel4 r Repetition Capture Flag Refer to the description of CC1RCFLG
15:13	Reserved		

14.6.6 Control event generation register (TMR3_CEG)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared by hardware. Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMR3_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared.
1	CC1EG	W	Capture/Compare Channel1 Event Generation 0: Invalid 1: Capture/Compare event is generated This bit is set to 1 by software and cleared automatically by hardware. **If Channel 1 is in output mode:** When CC1IFLG=1, if CC1IEN and CC1DEN bits are set, the corresponding interrupt and DMA request will be generated. **If Channel 1 is in input mode:** The value of the capture counter is stored in TMR3_CC1 register; configure CC1IFLG=1, and if CC1IEN and CC1DEN bits are also set, the corresponding interrupt and DMA request will be generated; at this time, if CC1IFLG=1, it is required to configure CC1RCFLG=1.
2	CC2EG	W	Capture/Compare Channel2 Event Generation Refer to CC1EG description
3	CC3EG	W	Capture/Compare Channel3 Event Generation Refer to CC1EG description
4	CC4EG	W	Capture/Compare Channel4 Event Generation Refer to CC1EG description
5	Reserved		
6	TEG	W	Trigger Event Generate 0: Invalid 1: Trigger event is generated This bit is set to 1 by software and cleared automatically by hardware.
15:8	Reserved		

14.6.7 Capture/Compare mode register 1 (TMR3_CCM1)

Offset address: 0x18

Reset value: 0x0000

The timer can be configured as input (capture mode) or output (compare mode) by CCxSEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output mode and input mode. The OCx in the register describes the function of the channel in the output mode, and the ICxx in the register describes the function of the channel in the input mode.

Output compare mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select This bit defines the input/output direction and the selected input pin. 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR3_CCEN register CC1EN=0).
2	OC1FEN	R/W	Output Compare Channel1 Fast Enable 0: Disable 1: Enable This bit is used to improve the response of the capture/compare output to the trigger input event.
3	OC1PEN	R/W	Output Compare Channel1 Preload Enable 0: Preloading function is disabled; write the value of TMR3_CC1 register through the program and it will work immediately. 1: Preloading function is enabled; write the value of TMR3_CC1 register through the program and it will work after an update event is generated. Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain.
6:4	OC1MOD	R/W	Output Compare Channel1 Mode Configure 000: Freeze The output compare has no effect on OC1REF 001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture/compareregister, OC1REF will be forced to be at high level 010: The output value is low when matching. When the value of the counter matches the value of the capture/compareregister, OC1REF will be forced to be at low level 011: Output flaps when matching. When the value of the counter matches the value of the capture/compareregister, flap the level of OC1REF 100: The output is forced to be ow Force OC1REF to be at low level 101: The output is forced to be high. Force OC1REF to be at high level 110: PWM mode 1 (set to high when the counter value<output compare value; otherwise, set to low) 111: PWM mode 2 (set to high when the counter value>output compare value; otherwise, set to low) Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the compare result changes or when the output compare mode changes from freeze mode to PWM mode.
7	OC1CEN	R/W	Output Compare Channel1 Clear Enable 0: OC1REF is unaffected by ETRF input. 1: When high level of ETRF input is detected, OC1REF=0
9:8	CC2SEL	R/W	Capture/Compare Channel2 Select This bit defines the input/output direction and the selected input pin. 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI2 10: CC2 channel is input, and IC2 is mapped on TI1 11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input

Field	Name	R/W	Description
			Note: This bit can be written only when the channel is disabled (TMR3_CCEN register CC2EN=0).
10	OC2FEN	R/W	Output Compare Channel2 Preload Enable Refer to the description of OC1FEN.
11	OC2PEN	R/W	Output Compare Channel2 Buffer Enable Refer to the description of OC1PEN.
14:12	OC2MOD	R/W	Output Compare Channel1 Mode Refer to the description of OC1MOD.
15	OC2CEN	R/W	Output Compare Channel2 Clear Enable Refer to the description of OC1CEN.

Input capture mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR3_CCEN bit CC1EN=0).
3:2	IC1PSC	R/W	Input Capture Channel 1 Perscaler Configure 00：PSC=1 01：PSC=2 10：PSC=4 11：PSC=8 PSC is prescaled factor, which triggers capture once every PSC events.
7:4	IC1F	R/W	Input Capture Channel 1 Filter Configure 0000: Filter disabled, sampling by f_{DTS} 0001：DIV=1，N=2 0010：DIV=1，N=4 0011：DIV=1，N=8 0100：DIV=2，N=6 0101：DIV=2，N=8 0110：DIV=4，N=6 0111：DIV=4，N=8 1000：DIV=8，N=6 1001：DIV=8，N=8 1010：DIV=16，N=5 1011：DIV=16，N=6 1100：DIV=16，N=8 1101：DIV=32，N=5 1110：DIV=32，N=6 1111：DIV=32，N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events.
9:8	CC2SEL	R/W	Capture/Compare Channel 2 Select 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI1 10: CC2 channel is input, and IC2 is mapped on TI2 11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR3_CCEN register CC2EN=0).

Field	Name	R/W	Description
11:10	IC2PSC	R/W	Input Capture Channel 2 Perscaler Configure Refer to the description of IC1PSC.
15:12	IC2F	R/W	Input Capture Channel 2 Filter Configure Refer to the description of IC1F.

14.6.8 Capture/Compare mode register 2 (TMR3_CCM2)

Offset address: 0x1C

Reset value: 0x0000

Refer to the description of the above CCM1 register.

Output compare mode:

Field	Name	R/W	Description
1:0	CC3SEL	R/W	Capture/Compare Channel 1 Select This bit defines the input/output direction and the selected input pin. 00: CC3 channel is output 01: CC3 channel is input, and IC3 is mapped on TI3 10: CC3 channel is input, and IC3 is mapped on TI4 11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR3_CCEN register CC3EN=0).
2	OC3FEN	R/W	Output Compare Channel3 Fast Enable Refer to the description of OC1FEN.
3	OC3PEN	R/W	Output Compare Channel3 Preload Enable Refer to the description of OC1PEN.
6:4	OC3MOD	R/W	Output Compare Channel3 Mode Configure Refer to the description of OC1MOD.
7	OC3CEN	R/W	Output Compare Channel3 Clear Enable Refer to the description of OC1CEN.
9:8	CC4SEL	R/W	Capture/Compare Channel 4 Select This bit defines the input/output direction and the selected input pin. 00: CC4 channel is output 01: CC4 channel is input, and IC4 is mapped on TI4 10: CC4 channel is input, and IC4 is mapped on TI3 11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR3_CCEN register CC4EN=0).
10	OC4FEN	R/W	Output Compare Channel4 Preload Enable Refer to the description of OC1FEN.
11	OC4PEN	R/W	Output Compare Channel4 Buffer Enable Refer to the description of OC1PEN.
14:12	OC4MOD	R/W	Output Compare Channel4 Mode Configure Refer to the description of OC1MOD.
15	OC4CEN	R/W	Output Compare Channel4 Clear Enable Refer to the description of OC1CEN.

Input capture mode:

Field	Name	R/W	Description
1:0	CC3SEL	R/W	Capture/Compare Channel 3 Select 00: CC3 channel is output 01: CC3 channel is input, and IC3 is mapped on TI3 10: CC3 channel is input, and IC3 is mapped on TI4

Field	Name	R/W	Description
			11: CC3 channel is input, and IC3 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR3_CCEN register CC3EN=0).
3:2	IC3PSC	R/W	Input Capture Channel 3 Perscaler Configure Refer to the description of IC1PSC.
7:4	IC3F	R/W	Input Capture Channel 3 Filter Configure Refer to the description of IC1F.
9:8	CC4SEL	R/W	Capture/Compare Channel 4 Select 00: CC4 channel is output 01: CC4 channel is input, and IC4 is mapped on TI4 10: CC4 channel is input, and IC4 is mapped on TI3 11: CC4 channel is input, and IC4 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR3_CCEN register CC4EN=0).
11:10	IC4PSC	R/W	Input Capture Channel 4 Perscaler Configure Refer to the description of IC1PSC.
15:12	IC4F	R/W	Input Capture Channel 4 Filter Configure Refer to the description of IC1F.

14.6.9 Capture/Compare enable register (TMR3_CCEN)

Offset address: 0x20

Reset value: 0x0000

Field	Name	R/W	Description
0	CC1EN	R/W	Capture/Compare Channel1 Output Enable **When the capture/compare channel 1 is configured as output:** 0: Output is disabled 1: Output is enabled **When the capture/compare channel 1 is configured as input:** This bit determines whether the value CNT of the counter can be captured and enter TMR3_CC1 register 0: Capture is disabled 1: Capture is enabled
1	CC1POL	R/W	Capture/Compare Channel1 Output Polarity Configure When CC1 channel is configured as output: 0: OC1 high level is valid 1: OC1 low level is valid When CC1 channel is configured as input: CC1POL and CC1NPOL control the polarity of the triggered or captured signals TI1FP1 and TI2FP1 at the same time 00: Non-phase-inverting/rising edge: TIxFP1 is not reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode). 01: Inverted phase/Falling edge: TIxFP1 is reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode). 10: Reserved 11: Non-phase-inverting/Rising and falling edges: TIxFP1 is not reversed phase (triggered in gated mode, cannot be used in encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode).

Field	Name	R/W	Description
2	Reserved		
3	CC1NPOL	R/W	Capture/Compare Channel1 Output Polarity Configure **When CC1 channel is configured as output:** CC1NPOL remains in cleared state all the time When CC1 channel is configured as input: Then CC1NPOL and CC1POL control the polarity of the triggered or captured signals TI1FP1 and TI2FP1 for the same time.
4	CC2EN	R/W	Capture/Compare Channel2 Output Enable Refer to the description of CC1EN
5	CC2POL	R/W	Capture/Compare Channel2 Output Polarity Configure Refer to the description of CC1POL
6	Reserved		
7	CC2NPOL	R/W	Capture/Compare Channel2 Output Polarity Configure Refer to the description of CC1NPOL
8	CC3EN	R/W	Capture/Compare Channel3 Output Enable Refer to the description of CC1EN
9	CC3POL	R/W	Capture/Compare Channel3 Output Polarity Configure Refer to the description of CC1POL
10	Reserved		
11	CC3NPOL	R/W	Capture/Compare Channel3 Output Polarity Configure Refer to the description of CC1NPOL
12	CC4EN	R/W	Capture/Compare Channel4 Output Enable Refer to the description of CC1EN
13	CC4POL	R/W	Capture/Compare Channel4 Output Polarity Configure Refer to the description of CC1POL
14	Reserved		
15	CC4NPOL	R/W	Capture/Compare Channel4 Output Polarity Configure Refer to the description of CC1NPOL

Table 48 Output Control Bit of Standard OCx Channel

CCxEN bit	OCx output state
0	Output is disabled (OCx=0, OCx_EN=0)
1	OCx=OCxREF+polarity, OCx_EN=1

Note: The state of external I/O pin connected to the standard OCx channel depends on the state of the OCx channel and the GPIO and AFIO registers.

14.6.10 Counter register (TMR3_CNT)

Offset address: 0x24

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CNT	R/W	Counter Value

14.6.11 Prescaler register (TMR3_PSC)

Offset address: 0x28

Reset value: 0x0000

Field	Name	R/W	Description
15:0	PSC	R/W	Prescaler Value Clock frequency of counter (CK_CNT)=f_{CK_PSC}/(PSC+1)

14.6.12 Auto reload register (TMR3_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF

Field	Name	R/W	Description
15:0	AUTORLD	R/W	Auto Reload Value When the value of auto reload is empty, the counter will not count.

14.6.13 Channel 1 capture/compare register (TMR3_CC1)

Offset address: 0x34

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC1	R/W	Capture/Compare Channel 1 Value **When the capture/compare channel 1 is configured as input mode:** CC1 contains the counter value transmitted by the last input capture channel 1 event. **When the capture/compare channel 1 is configured as output mode:** CC1 contains the current load capture/compare register value Compare the value CC1 of the capture and compare channel 1 with the value CNT of the counter to generate the output signal on OC1. When the output compare preload is disabled (OC1PEN=0 for TMR3_CCM1 register), the written value will immediately affect the output compare results; If the output compare preload is enabled (OC1PEN=1 for TMR3_CCM1 register), the written value will affect the output compare result when an update event is generated.

14.6.14 Channel 2 capture/compare register (TMR3_CC2)

Offset address: 0x38

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC2	R/W	Capture/Compare Channel 2 Value Refer to the description of TMR3_CC1

14.6.15 Channel 3 capture/compare register (TMR3_CC3)

Offset address: 0x3C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC3	R/W	Capture/Compare Channel 3 Value Refer to the description of TMR3_CC1

14.6.16 Channel 4 capture/compare register (TMR3_CC4)

Offset address: 0x40

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC4	R/W	Capture/Compare Channel 4 Value Refer to the description of TMR3_CC1

14.6.17 DMA control software (TMR3_DCTRL)

Offset address: 0x48

Reset value: 0x0000

Field	Name	R/W	Description
4:0	DBADDR	R/W	DMA Base Address Setup These bits define the base address of DMA in continuous mode (when reading or writing TMR3_DMADDR register), and DBADDR is defined as the offset from the address of TMR3_CTRL1 register: 00000：TMR3_CTRL1 00001：TMR3_CTRL2 00010：TMR3_SMCTRL …….
7:5	Reserved		
12:8	DBLEN	R/W	DMA Burst Transfer Length Setup These bits define the transfer length and transfer times of DMA in continuous mode. The data transferred can be 16 bits and 8 bits. When reading/writing TMR3_DMADDR register, the timer will conduct a continuous transmission; 00000: Transmission for 1 time 00001: Transmission for 2 times 00010: Transmission for 3 times …… 10001: Transmission for 18 times The transmission address formula is as follows: Transmission address=TMR3_CTRL1 address (slave address) +DBADDR+DMA index; DMA index=DBLEN For example: DBLEN=7, DBADDR=TMR3_CTRL1 (slave address) means the address of the data to be transmitted, while the address +DBADDR+7 of TMR3_CTRL1 means the address of the data to be written/read, Data transmission will occur to: TMR3_CTRL1 address + seven registers starting from DBADDR. The data transmission will change according to different DMA data length: (1) When the transmission data is set to 16 bits, the data will be transmitted to seven registers (2) When the transmission data is set to 8 bits, the data of the first register is the MSB bit of the first data, the data of the second register is the LSB bit of the first data, and the data will still be transmitted to seven registers.
15:13	Reserved		

14.6.18 DMA address register of continuous mode (TMR3_DMADDR)

Offset address: 0x4C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	DMADDR	R/W	DMA Register for Burst Transfer Read or write operation access of TMR3_DMADDR register may lead to access operation of the register in the following address: TMR3_CTRL1 address + (DBADDR+DMA index) ×4 Wherein: "TMR3_CTRL1 address" is the address of control register 1 (TMR3_CTRL1); "DBADDR" is the base address defined in TMR3_DCTRL register; "DMA index" is the offset automatically controlled by DMA, and it depends on DBLEN defined in TMR3_DCTRL register.

15 General-purpose Timer (TMR14)

15.1 Introduction

The general-purpose timer takes the time base unit as the core, and has the functions of input capture and output compare, and can be used to measure the pulse width, frequency and duty cycle, and generate the output waveform. It includes a 16-bit auto reload counter (realize count-up).

15.2 Main Characteristics

（1） Timebase unit
- Counter: 16-bit counter, which can only count up
- Prescaler: 16-bit programmable prescaler
- Auto reloading function

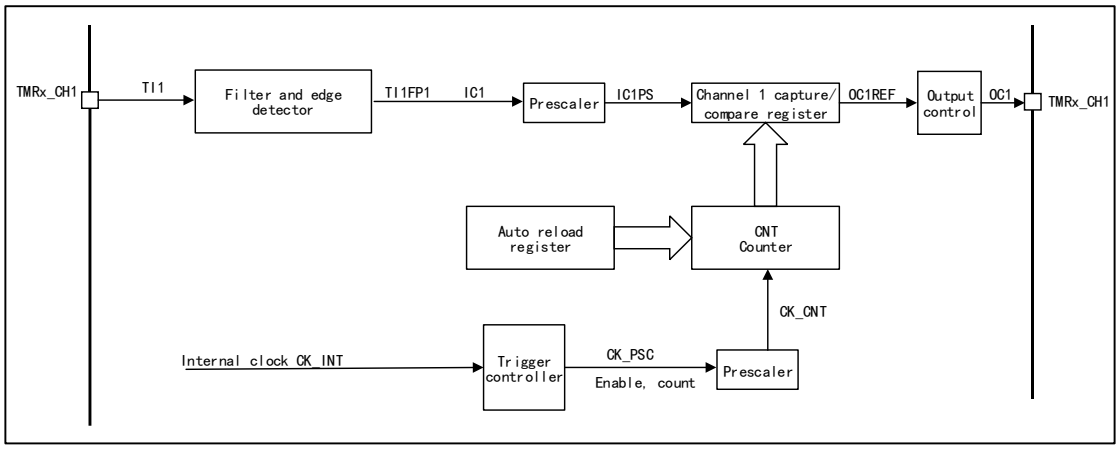
（2） Clock source
- Internal clock

（3） Timer function
- Input capture
- Output compare
- PWM output mode
- Forced output mode

（4） Interrupt event
- Update event (counter overrun, counter initialization)
- Input capture
- Output compare

15.3 Structure Block Diagram

Figure 60 General-purpose Timer TMR14 Structure Block Diagram



15.4 Functional Description

15.4.1 Clock Source

Internal clock

It is TMR14_CLK from RCM, namely the driving clock of the timer; when the slave mode controller is disabled, the clock source CK_PSC of the prescaler is driven by the internal clock CK_INT.

15.4.2 Timebase Unit

The time base unit in the general-purpose timer contains three registers

- Counter register (CNT) 16 bits
- Auto reload register (AUTORLD) 16 bits
- Prescaler register (PSC) 16 bits

Counter CNT

The counter in the general-purpose timer can only count-up

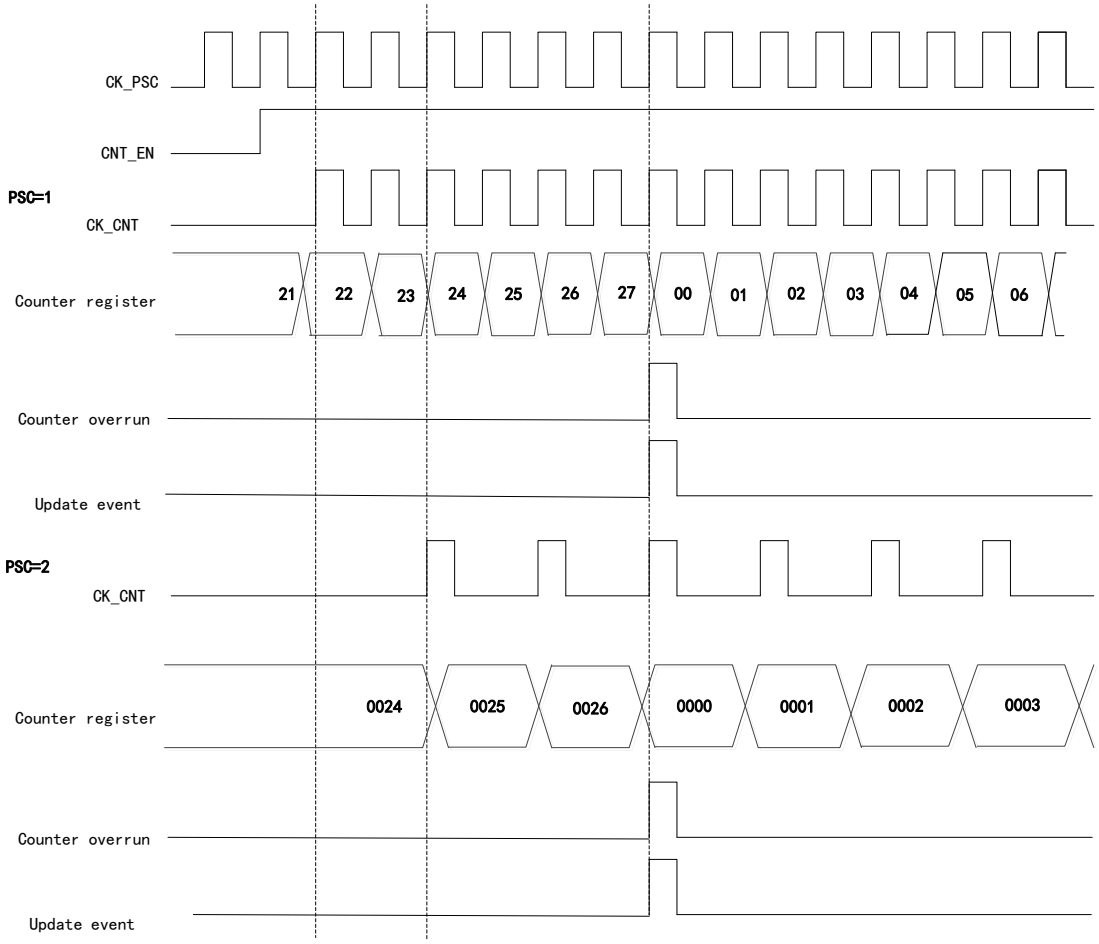
Count-up mode

When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMR14_CNT) is equal to the value of the auto reload (TMR14_AUTORLD), the counter will start to count again from 0, a count-up overrun event will be generated, and the value of the auto reload (TMR14_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the auto reload register and the prescaler register will be updated. The update event can be disabled by UD bit of configuration control register TMR14_CTRL1.

The figure below is Timing Diagram when Division Factor is 1 or 2 in Count-up Mode

Figure 61 Timing Diagram when Division Factor is 1 or 2 in Count-up Mode



Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value between 1 and 65536 (controlled by TMR14_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

15.4.3 Input Capture

Input capture channel

The general-purpose timer has one independent capture/compare channels, each of which is surrounded by a capture/compare register.

In the input capture, the measured signal will enter from the external pin T1 of the timer, first pass through the edge detector and input filter, and then into the capture channel. Each capture channel has a corresponding capture register. When the capture occurs, the value of the counter CNT will be latched in the capture register CCx. Before entering the capture register, the signal will pass through the prescaler, which is used to set how many events to capture at a time.

Input capture application

Input capture is used to capture external events, and can give the time flag to indicate the occurrence time of the event and measure the pulse jump edge

events (measure the frequency or pulse width), for example, if the selected edge appears on the input pin, the TMR14_CCx register will capture the current value of the counter and the CCxIFLG bit of the state register TMR14_STS will be set to 1; if CCxIEN=1, an interrupt will be generated.

In capture mode, the timing, frequency, period and duty cycle of a waveform can be measured. In the input capture mode, the edge selection is set to rising edge detection. When the rising edge appears on the capture channel, the first capture occurs, at this time, the value of the counter CNT will be latched in the capture register CCx; at the same time, it will enter the capture interrupt, a capture will be recorded in the interrupt service program and the value will be recorded. When the next rising edge is detected, the second capture occurs, the value of counter CNT will be latched in capture register CCx again, at this time, it will enter the capture interrupt again, the value of capture register will be read, and the cycle of this pulse signal will be obtained through capture.

15.4.4 Output Compare

There are eight modes of output compare: freeze, channel x is valid level when matching, channel x is invalid level when matching, flip, force is invalid, force is valid, PWM1 and PWM2 modes, which are configured by OCxMOD bit in TMR14_CCMx register and can control the waveform of output signal in output compare mode.

Output compare application

In the output compare mode, the position, polarity, frequency and time of the pulse generated by the timer can be controlled.

When the value of the counter is equal to that of the capture/compare register, the channel output can be set as high level, low level or flip by configuring the OCxMOD bit in TMR14_CCMx register and the CCxPOL bit in the output polarity TMR14_CCEN register.

When CCxIFLG=1 in TMR14_STS register, if CCxIEN=1 in TMR14_DIEN register, an interrupt will be generated.

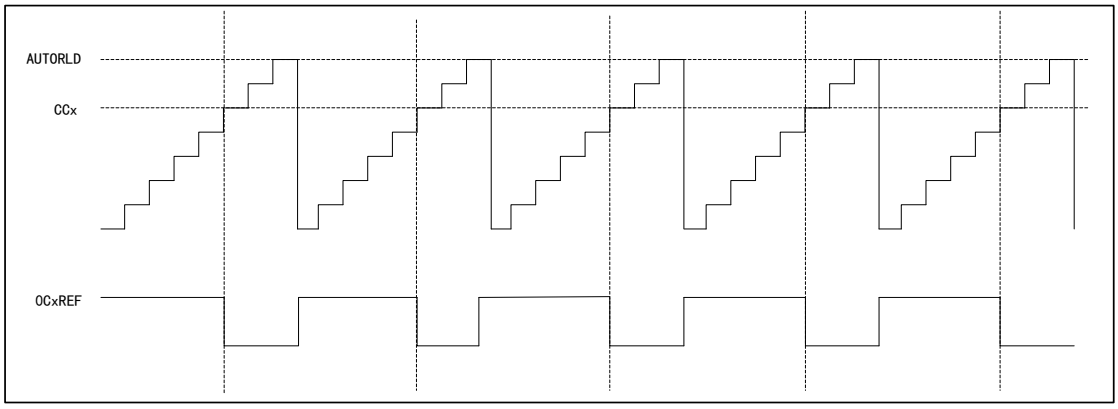
15.4.5 PWM Output Mode

PWM mode is an adjustable pulse signal output by the timer. The pulse width of the signal is determined by the value of the compare register CCx, and the cycle is determined by the value of the auto reload AUTORLD.

PWM output mode contains PWM mode 1 and PWM mode 2; PWM mode 1 and PWM mode 2 can only count-up.

Set the timing diagram in PWM mode 1 when CCx=5, AUTORLD=7

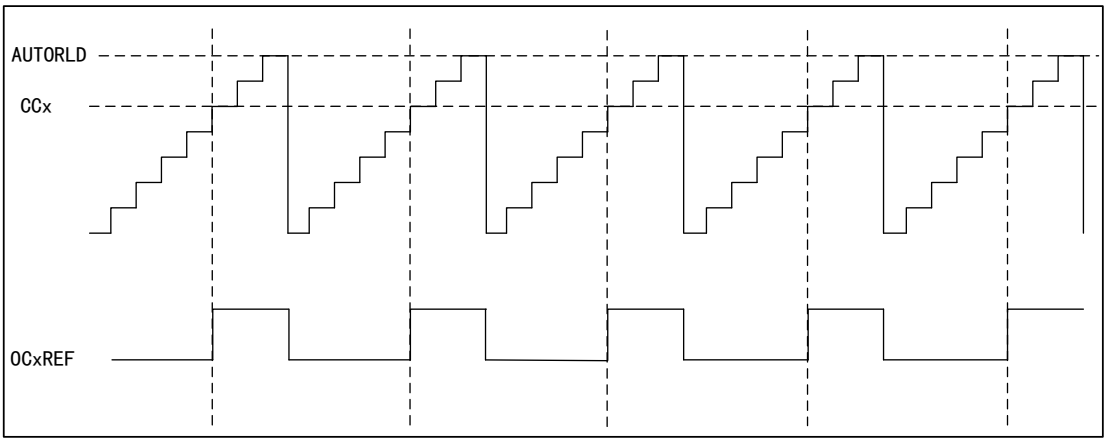
Figure 62 PWM1 Count-up Mode Timing Diagram



In PWM mode 2, if the value of the counter CNT is less than that of the compare register CCx, the output level will be invalid; otherwise, it will be valid.

Set the timing diagram in PWM mode 2 when CCx=5, AUTORLD=7

Figure 63 PWM2 Count-up Mode Timing Diagram



15.4.6 Forced Output Mode

In the forced output mode, the compare result is ignored, and the corresponding level is directly output according to the configuration instruction.

- CCxSEL=00 for TMR14_CCMx register, set CCx channel as output
- OCxMOD=100/101 for TMR14_CCMx register, set to force OCxREF signal to invalid/valid state

In this mode, the corresponding interrupt will still be generated.

15.5 Register Address Mapping

In the following table, all registers of TMR14 are mapped to a 16-bit addressable (address) space.

Table 49 TMR14 Register Address Mapping

Register name	Description	Offset address
TMR14_CTRL1	Control register 1	0x00

Register name	Description	Offset address
TMR14_DIEN	DMA/Interrupt enable register	0x0C
TMR14_STS	State register	0x10
TMR14_CEG	Control event generation register	0x14
TMR14_CCM1	Capture/Compare mode register 1	0x18
TMR14_CCEN	Capture/Compare enable register	0x20
TMR14_CNT	Counter register	0x24
TMR14_PSC	Prescaler register	0x28
TMR14_AUTORLD	Auto reload register	0x2C
TMR14_CC1	Channel 1 capture/compare register	0x34
TMR14_OPT	Option register	0x50

15.6 Register Functional Description

15.6.1 Control register 1 (TMR14_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.
1	UD	R/W	Update Disable Update event can cause AUTORLD, PSC and CCx to generate the value of update setting. 0: Update event is allowed (UEV) An update event can occur in any of the following situations: The counter overruns; Set UEG bit; Updates generated from the schema controller. 1: Update event is disabled
2	URSSEL	R/W	Update Request Source Select If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit. 0: The counter overruns; Set UEG bit; 1: The counter overruns
6:3	Reserved		
7	ARPEN	R/W	Auto-reload Preload Enable When the buffer is disabled, the program modification TMR14_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMR14_AUTORLD will modify the values loaded to the counter in the next update event. 0: Disable 1: Enable
9:8	CLKDIV	R/W	Clock Divide Factor

Field	Name	R/W	Description
			For the configuration of dead time and digital filter, CK_INT provides the clock, and the dead time and the clock of the digital filter can be adjusted by setting this bit. 00：$t_{DTS}=t_{CK\_INT}$ 01：$t_{DTS}=2\times t_{CK\_INT}$ 10：$t_{DTS}=4\times t_{CK\_INT}$ 11: Reserved
15:10	Reserved		

15.6.2 DMA/Interrupt enable register (TMR14_DIEN)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
0	UIEN	R/W	Update interrupt Enable 0: Disable 1: Enable
1	CC1IEN	R/W	Capture/Compare Channel1 Interrupt Enable 0: Disable 1: Enable
15:2	Reserved		

15.6.3 State register (TMR14_STS)

Offset address: 0x10

Reset value: 0x0000

Field	Name	R/W	Description
0	UIFLG	RC_W0	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur 1: Update event interrupt occurs When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations: (1) UD=0 on TMR14_CTRL1 register, and when overruns an update event will be generated; (2) URSSEL=0 and UD=0 on TMR14_CTRL1 register, configure UEG=1 on TMR14_CEG register to generate update event, and the counter needs to be initialized by software;
1	CC1IFLG	RC_W0	Capture/Compare Channel1 Interrupt Flag **When the capture/compare channel 1 is configured as output:** 0: No matching occurred 1: The value of TMR14_CNT matches the value of TMR14_CC1 **When the capture/compare channel 1 is configured as input:** 0: Input capture did not occur 1: Input capture occurred When a capture event occurs, the bit is set to 1 by hardware, and it can be cleared by software or cleared when reading TMR14_CC1 register.
8:7	Reserved		
9	CC1RCFLG	RC_W0	Capture/compare Channel1 Repetition Capture Flag 0: Repeat capture does not occur 1: Repeat capture occurs The value of the counter is captured to TMR14_CC1 register, and CC1IFLG=1; this bit is set to 1 by hardware and cleared by software only when the channel is configured as input capture.
15:10	Reserved		

15.6.4 Control event generation register (TMR14_CEG)

Offset address: 0x14
Reset value: 0x0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared by hardware. Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In count-up mode, the counter will be cleared.
1	CC1EG	W	Capture/Compare Channel1 Event Generation 0: Invalid 1: Capture/Compare event is generated This bit is set to 1 by software and cleared automatically by hardware. **If Channel 1 is in output mode:** When CC1IFLG=1, if CC1IEN bits are set, the corresponding interrupt and DMA request will be generated. **If Channel 1 is in input mode:** The value of the capture counter is stored in TMR14_CC1 register; configure CC1IFLG=1, and if CC1IEN bits are also set, the corresponding interrupt and DMA request will be generated; at this time, if CC1IFLG=1, it is required to configure CC1RCFLG=1.
15:2	Reserved		

15.6.5 Capture/Compare mode register 1 (TMR14_CCM1)

Offset address: 0x18
Reset value: 0x0000

The timer can be configured as input (capture mode) or output (compare mode) by CCxSEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output mode and input mode. The OCx in the register describes the function of the channel in the output mode, and the ICxx in the register describes the function of the channel in the input mode.

Output compare mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select This bit defines the input/output direction and the selected input pin. 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 1x: Reserve Note: This bit can be written only when the channel is disabled (TMR14_CCEN register CC1EN=0).
2	OC1FEN	R/W	Output Compare Channel1 Fast Enable 0: Disable 1: Enable This bit is used to improve the response of the capture/compare output to the trigger input event.
3	OC1PEN	R/W	Output Compare Channel1 Preload Enable 0: Preloading function is disabled; write the value of TMR14_CC1 register through the program and it will work immediately. 1: Preloading function is enabled; write the value of TMR14_CC1 register through the program and it will work after an update event is generated. Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain.
6:4	OC1MOD	R/W	Output Compare Channel1 Mode Configure 000: Freeze The output compare has no effect on OC1REF

Field	Name	R/W	Description
			001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture/compareregister, OC1REF will be forced to be at high level 010: The output value is low when matching. When the value of the counter matches the value of the capture/compareregister, OC1REF will be forced to be at low level 011: Output flaps when matching. When the value of the counter matches the value of the capture/compareregister, flap the level of OC1REF 100: The output is forced to be ow Force OC1REF to be at low level 101: The output is forced to be high. Force OC1REF to be at high level 110: PWM mode 1 (set to high when the counter value<output compare value; otherwise, set to low) 111: PWM mode 2 (set to high when the counter value>output compare value; otherwise, set to low) Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the compare result changes or when the output compare mode changes from freeze mode to PWM mode.
15:7	Reserved		

Input capture mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 1x: Reserve Note: This bit can be written only when the channel is disabled (TMR14_CCEN register CC1EN=0).
3:2	IC1PSC	R/W	Input Capture Channel 1 Perscaler Configure 00：PSC=1 01：PSC=2 10：PSC=4 11：PSC=8 PSC is prescaled factor, which triggers capture once every PSC events.
7:4	IC1F	R/W	Input Capture Channel 1 Filter Configure 0000: Filter disabled, sampling by f_{DTS} 0001：DIV=1，N=2 0010：DIV=1，N=4 0011：DIV=1，N=8 0100：DIV=2，N=6 0101：DIV=2，N=8 0110：DIV=4，N=6 0111：DIV=4，N=8 1000：DIV=8，N=6 1001：DIV=8，N=8 1010：DIV=16，N=5 1011：DIV=16，N=6 1100：DIV=16，N=8 1101：DIV=32，N=5 1110：DIV=32，N=6 1111：DIV=32，N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events.
15:8	Reserved		

15.6.6 Capture/Compare enable register (TMR14_CCEN)

Offset address: 0x20

Reset value: 0x0000

Field	Name	R/W	Description
0	CC1EN	R/W	Capture/Compare Channel1 Output Enable **When the capture/compare channel 1 is configured as output:** 0: Output is disabled 1: Output is enabled **When the capture/compare channel 1 is configured as input:** This bit determines whether the value CNT of the counter can be captured and enter TMR14_CC1 register 0: Capture is disabled 1: Capture is enabled
1	CC1POL	R/W	Capture/Compare Channel1 Output Polarity Configure When CC1 channel is configured as output: 0: OC1 high level is valid 1: OC1 low level is valid When CC1 channel is configured as input: CC1POL and CC1NPOL control the polarity of the triggered or captured signals TI1FP1 and TI2FP1 at the same time 00: Non-phase-inverting/rising edge: TIxFP1 is not reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode). 01: Inverted phase/Falling edge: TIxFP1 is reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode). 10: Reserved 11: Non-phase-inverting/Rising and falling edges: TIxFP1 is not reversed phase (triggered in gated mode, cannot be used in encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode).
2	Reserved		
3	CC1NPOL	R/W	Capture/Compare Channel1 Output Polarity Configure **When CC1 channel is configured as output:** CC1NPOL remains in cleared state all the time When CC1 channel is configured as input: Then CC1NPOL and CC1POL control the polarity of the triggered or captured signals TI1FP1 and TI2FP1 for the same time.
15:4	Reserved		

Table 50 Output Control Bit of Standard OCx Channel

CCxEN bit	OCx output state
0	Output is disabled (OCx=0, OCx_EN=0)
1	OCx=OCxREF+polarity, OCx_EN=1

Note: The state of external I/O pin connected to the standard OCx channel depends on the state of the OCx channel and the GPIO and AFIO registers.

15.6.7 Counter register (TMR14_CNT)

Offset address: 0x24

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CNT	R/W	Counter Value

15.6.8 Prescaler register (TMR14_PSC)

Offset address: 0x28

Reset value: 0x0000

Field	Name	R/W	Description
15:0	PSC	R/W	Prescaler Value Clock frequency of counter (CK_CNT)=f_{CK_PSC}/(PSC+1)

15.6.9 Auto reload register (TMR14_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF

Field	Name	R/W	Description
15:0	AUTORLD	R/W	Auto Reload Value When the value of auto reload is empty, the counter will not count.

15.6.10 Channel 1 capture/compare register (TMR14_CC1)

Offset address: 0x34

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC1	R/W	Capture/Compare Channel 1 Value **When the capture/compare channel 1 is configured as input mode:** CC1 contains the counter value transmitted by the last input capture channel 1 event. **When the capture/compare channel 1 is configured as output mode:** CC1 contains the current load capture/compare register value Compare the value CC1 of the capture and compare channel 1 with the value CNT of the counter to generate the output signal on OC1. When the output compare preload is disabled (OC1PEN=0 for TMR14_CCM1 register), the written value will immediately affect the output compare results; If the output compare preload is enabled (OC1PEN=1 for TMR14_CCM1 register), the written value will affect the output compare result when an update event is generated.

15.6.11 Option register (TMR14_OPT)

Offset address: 0x50

Reset value: 0x0000

Field	Name	R/W	Description
1:0	RMPSEL	R/W	Timer Input 1 Remap Select 00: TMR14 channel 1 is connected to the GPIO multiplexing pin. Refer to Data Manual 3.3 Multiplexing List. 01: TMR14 channel 1 is connected to RTCCLK 10: TMR14 channel 1 is connected to HSECLK/32 11: TMR14 channel 1 is connected to the main clock output (MCO), which is selected by MCOSEL bit of the clock configuration register RCM_CFG1.
15:2	Reserved		

16 General-purpose Timer (TMR15/16/17)

16.1 Introduction

The general-purpose timer takes the time base unit as the core, and has the functions of input capture and output compare, and can be used to measure the pulse width, frequency and duty cycle, and generate the output waveform. It includes a 16-bit auto reload counter (realize count-up, count-down and center-aligned count). It supports complementary output, repeat count and programmable dead-time insertion function, and is more suitable for motor control.

16.2 Main Characteristics

（1） Timebase unit

- Counter: 16-bit counter, which can only count up
- Prescaler: 16-bit programmable prescaler
- Repeat counter: 16-bit repeat counter
- Auto reloading function

（2） Clock source selection

- Internal clock
- External input (only applicable to TMR15)
- Internal trigger (only applicable to TMR15)

（3） Input Capture function

- Counting function
- PWM input mode (only applicable to TMR15)

（4） Output Compare function

- PWM output mode
- Forced output mode
- Single-pulse mode
- Complementary output and dead-time insertion

（5） Breaking function

（6） Master/Slave mode controller of timer (only applicable to TMR15)

- Timers can be synchronized and cascaded
- Support multiple slave modes and synchronization signals

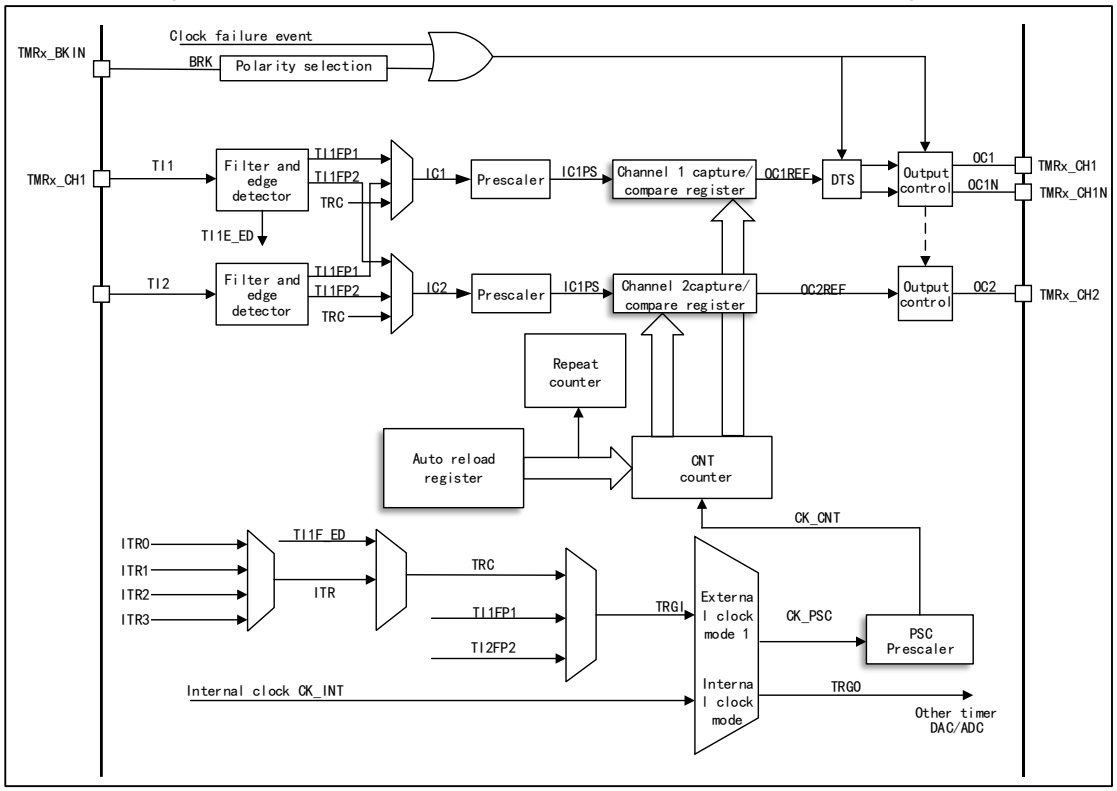
（7） Interrupt output and DMA request event

- Update event (counter overrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Compare event
- Breaking signal input event

16.3 Structure Block Diagram

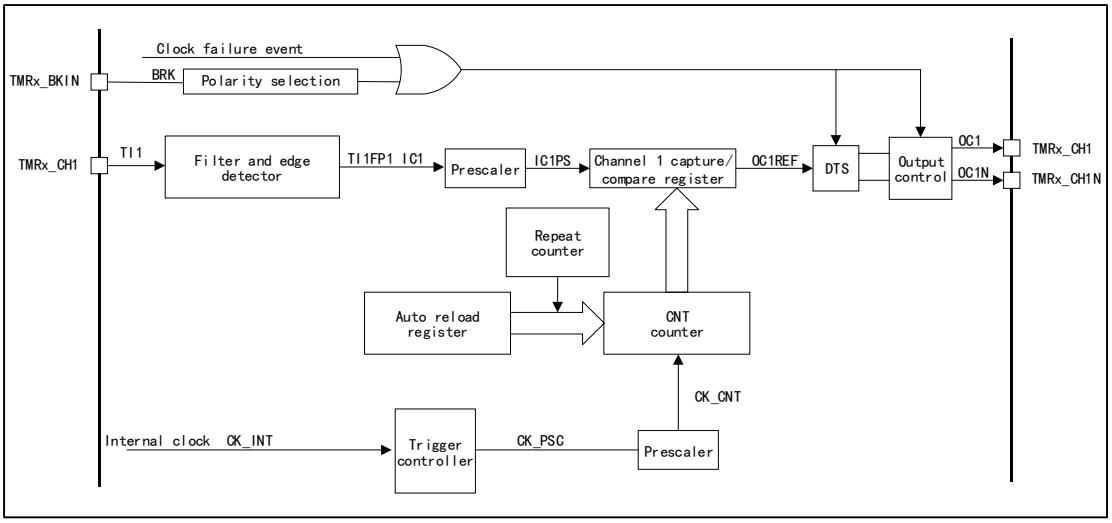
16.3.1 General-purpose Timer TMR15 Structure Block Diagram

Figure 64 General-purpose Timer TMR15 Structure Block Diagram



16.3.2 General-purpose Timer TMR16/17 Structure Block Diagram

Figure 65 General-purpose Timer TMR16/17 Structure Block Diagram



16.4 Functional Description

16.4.1 Clock Source Selection

The general-purpose timer has four clock sources

Internal clock

It is TMRx_CLK from RCM, namely the driving clock of the timer; when the slave mode controller is disabled, the clock source CK_PSC of the prescaler is driven by the internal clock CK_INT.

External clock mode 1 (TMR15)

The trigger signal generated from the input channel TI1/2/3/4 of the timer after polarity selection and filtering is connected to the slave mode controller to control the work of the counter. Besides, the pulse signal generated by the input of Channel 1 after double-edge detection of the rising edge and the falling edge is logically equal or the future signal is TI1F_ED signal, namely double-edge signal of TIF_ED. Specially the PWM input can only be input by TI1/2.

Internal trigger input (only applicable to TMR15)

The timer is set to work in slave mode, and the clock source is the output signal of other timers. At this time, the clock source has no filtering, and the synchronization or cascading between timers can be realized. The master mode timer can reset, start, stop or provide clock for the slave mode timer.

16.4.2 Timebase Unit

The time base unit in the general-purpose timer contains four registers

- Counter register (CNT) 16 bits
- Auto reload register (AUTORLD) 16 bits
- Prescaler register (PSC) 16 bits
- Repetition count register (REPCNT) 8 bits

Counter CNT

The counters of TMR15/16/17 timers can only count up.

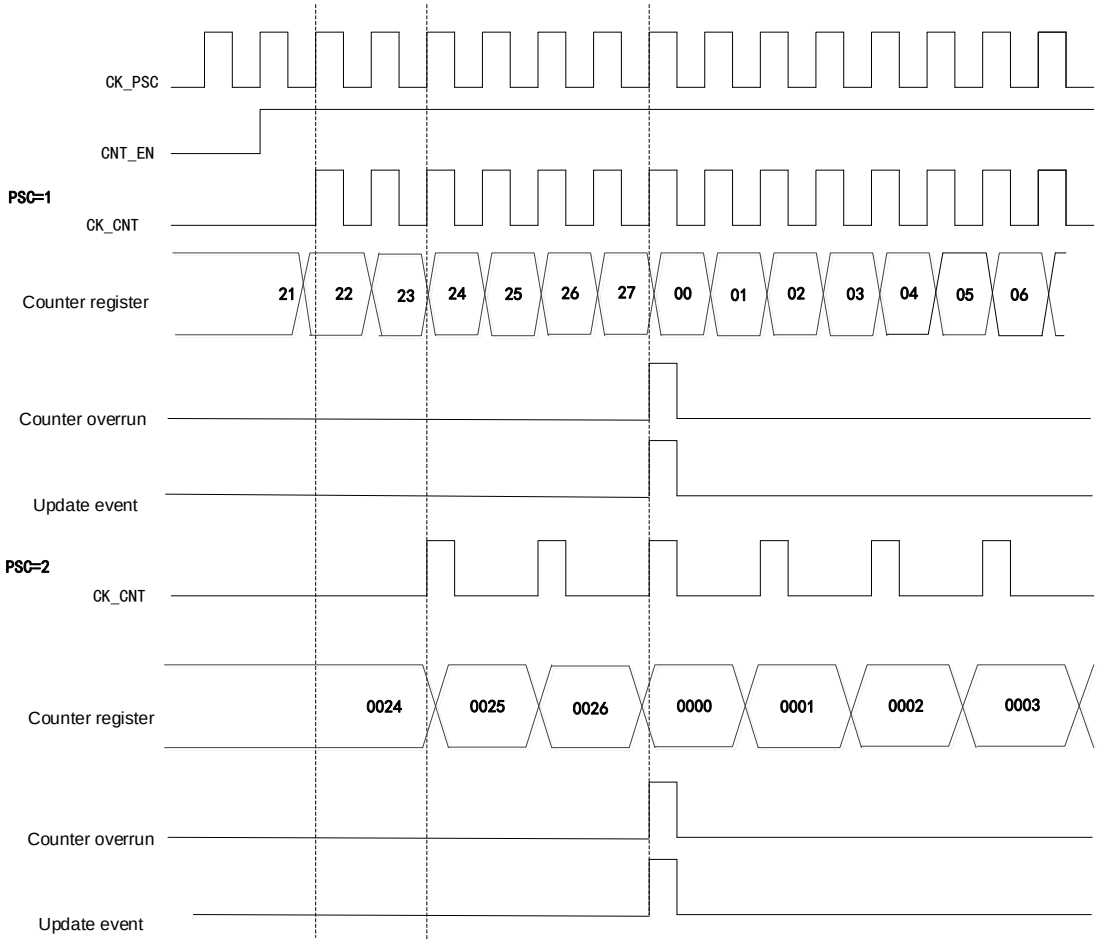
Count-up mode

When the counter is in count-up mode, the counter will count up from 0; every time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMRx_CNT) is equal to the value of the auto reload (TMRx_AUTORLD), the counter will start to count again from 0, a count-up overrun event will be generated, and the value of the auto reload (TMRx_AUTORLD) is written in advance.

When the counter overruns, an update event will be generated. At this time, the repeat count shadow register, the auto reload shadow register and the prescaler buffer will be updated. The update event can be disabled by UD bit of configuration control register TMRx_CTRL1.

The figure below is Timing Diagram when Division Factor is 1 or 2 in Count-up Mode

Figure 66 Timing Diagram when Division Factor is 1 or 2 in Count-up Mode



Repetition counter REPCNT

There is has repeat counter REPCNT in the general-purpose timer TMR15/16/17, when an overrun/unerrrun event occurs to the general-purpose timer, the update event will be generated only when the value of the repeat counter is 0.

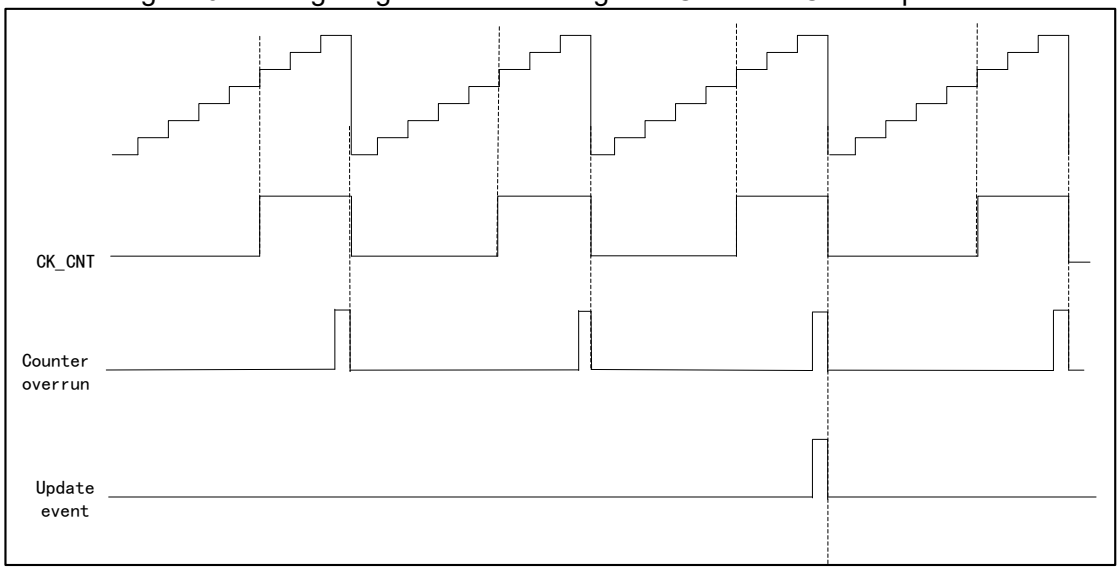
For example, if the general-purpose timer TMR15/16/17 needs to generate an update event when an overrun/underrun event occurs, the value of the repeat counter should be set to 0.

If the repeat counter function is used in the count-up mode, every time the counter counts up to AUTORLD, an overrun event will occur. At this time, the value of the repeat counter will be decreased by 1, and an update event will be generated until the value of the repeat counter is 0.

That is, when N+1 (N is the value of repeat counter) overrun/underrun events occur, an update event will be generated.

The figure below shows the Timing Diagram when Setting REPCNT=2 in Count-up Mode

Figure 67 Timing Diagram when Setting REPCNT=2 in Count-up Mode



Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value between 1 and 65536 (controlled by TMRx_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

16.4.3 Input Capture

Input capture channel

The general-purpose timer has two independent capture/compare channels (TMR16/17 only one), each of which is surrounded by a capture/compare register. In the input capture, the measured signal will enter from the external pin T1/2/3/4 of the timer, first pass through the edge detector and input filter, and then into the capture channel. Each capture channel has a corresponding capture register. When the capture occurs, the value of the counter CNT will be latched in the capture register CCx. Before entering the capture register, the signal will pass through the prescaler, which is used to set how many events to capture at a time.

Input capture application

Input capture is used to capture external events, and can give the time flag to indicate the occurrence time of the event and measure the pulse jump edge events (measure the frequency or pulse width), for example, if the selected edge appears on the input pin, the TMRx_CCx register will capture the current value of the counter and the CCxIFLG bit of the state register TMRx_STS will be set to 1; if CCxIEN=1, an interrupt will be generated.

In capture mode, the timing, frequency, period and duty cycle of a waveform can be measured. In the input capture mode, the edge selection is set to rising edge detection. When the rising edge appears on the capture channel, the first capture occurs, at this time, the value of the counter CNT will be latched in the capture register CCx; at the same time, it will enter the capture interrupt, a capture will be recorded in the interrupt service program and the value will be recorded. When the next rising edge is detected, the second capture occurs, the value of counter CNT will be latched in capture register CCx again, at this time, it will enter the capture interrupt again, the value of capture register will be read, and the cycle of this pulse signal will be obtained through capture.

16.4.4 Output Compare

There are eight modes of output compare: freeze, channel x is valid level when matching, channel x is invalid level when matching, flip, force is invalid, force is

valid, PWM1 and PWM2 modes, which are configured by OCxMOD bit in TMRx_CCMx register and can control the waveform of output signal in output compare mode.

Output compare application

In the output compare mode, the position, polarity, frequency and time of the pulse generated by the timer can be controlled.

When the value of the counter is equal to that of the capture/compare register, the channel output can be set as high level, low level or flip by configuring the OCxMOD bit in TMRx_CCMx register and the CCxPOL bit in the output polarity TMRx_CCEN register.

When CCxIFLG=1 in TMRx_STS register, if CCxIEN=1 in TMRx_DIEN register, an interrupt will be generated; if CCDSEL=1 in TMRx_CTRL2 register, DMA request will be generated.

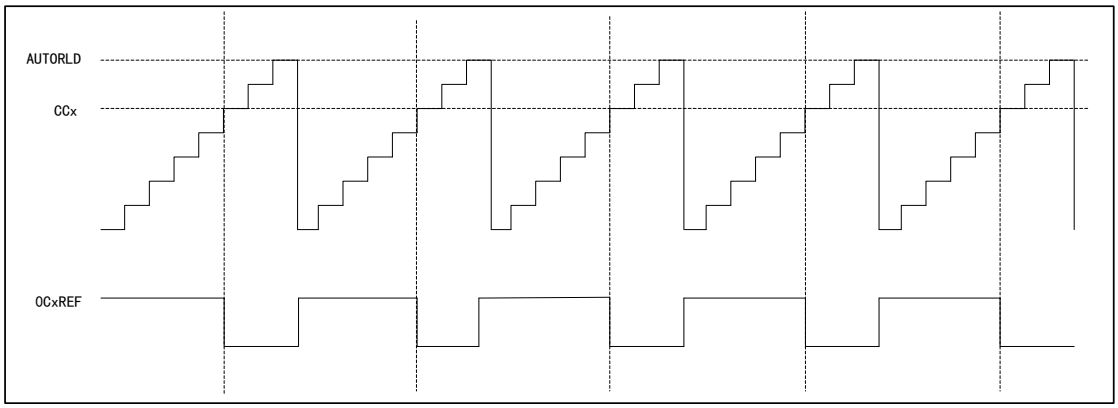
16.4.5 PWM Output Mode

PWM mode is an adjustable pulse signal output by the timer. The pulse width of the signal is determined by the value of the compare register CCx, and the cycle is determined by the value of the auto reload AUTORLD.

PWM output mode contains PWM mode 1 and PWM mode 2; PWM mode 1 and PWM mode 2 can only count-up.In PWM mode 1, if the value of the counter CNT is less than the value of the compare register CCx, the output level will be valid; otherwise, it will be invalid.

Set the timing diagram in PWM mode 1 when CCx=5, AUTORLD=7

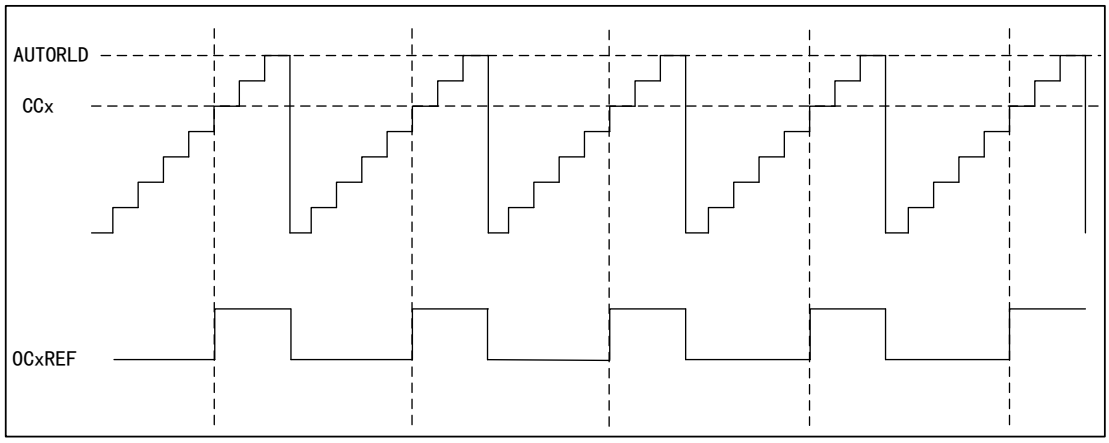
Figure 68 PWM1 Count-up Mode Timing Diagram



In PWM mode 2, if the value of the counter CNT is less than that of the compare register CCx, the output level will be invalid; otherwise, it will be valid.

Set the timing diagram in PWM mode 2 when CCx=5, AUTORLD=7

Figure 69 PWM2 Count-up Mode Timing Diagram



16.4.6 PWM Input Mode (only applicable to TMR15)

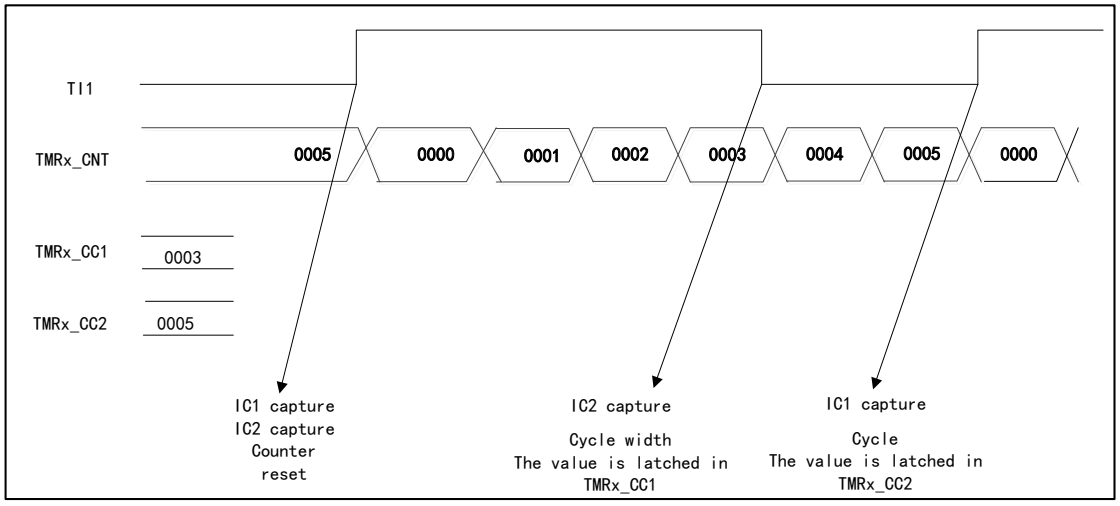
PWM input mode is a particular case of input capture.

In PWM input mode, as only TI1FP1 and TI1FP2 are connected to the slave mode controller, input can be performed only through the channels TMR15_CH1 and TMR15_CH2, which need to occupy the capture registers of CH1 and CH2.

In the PWM input mode, the PWM signal enters from TMR15_CH1, and the signal will be divided into two channels, one can measure the cycle and the other can measure the duty cycle. In the configuration, it is only required to set the polarity of one channel, and the other will be automatically configured with the opposite polarity.

In this mode, the slave mode controller should be configured as the reset mode (SMFSEL bit of TMR15_SMCTRL register)

Figure 70 Timing Diagram in PWM Input Mode



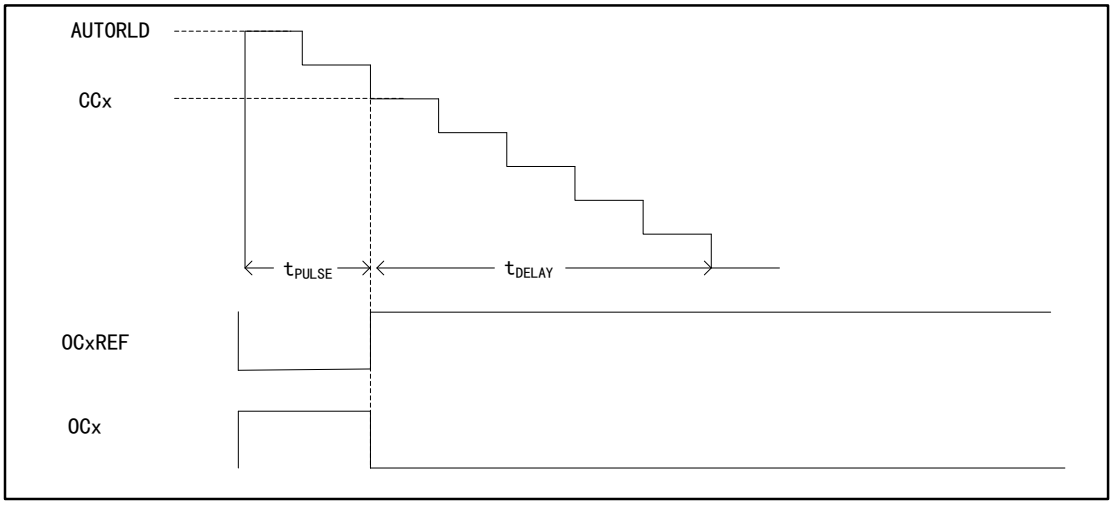
16.4.7 Single-pulse Mode

The single-pulse mode is a special case of timer compare output, and is also a special case of PWM output mode.

Set SPMEN bit of TMRx_CTRL1 register, and select the single-pulse mode. After the counter is started, a certain number of pulses will be output before the update event occurs. When an update event occurs, the counter will stop counting, and the subsequent PWM waveform output will no longer be changed.

After a certain controllable delay, a pulse with controllable pulse width is generated in single-pulse mode through the program. The delay time is defined by the value of TMRx_CCx register; in the count-up mode, the delay time is CCx and the pulse width is AUTORLD-CCx; in the count-down mode, the delay time is AUTORLD-CCx and the pulse width is CCx.

Figure 71 Timing Diagram in Single-pulse Mode



16.4.8 Impact of the Register on Output Waveform

The following registers will affect the level of the timer output waveform. For details, please refer to "Register Functional Description".

（1） CCxEN and CCxNEN bits in TMRx_CCEN register
- CCxNEN=0 and CCxEN=0: The output is turned off (output disabled, invalid state)
- CCxNEN=1 and CCxEN=1: The output is turned on (output enabled, normal output)

（2） MOEN bit in TMRx_BDT register
- MOEN=0: Idle mode
- MOEN=1: Run mode

（3） OCxOIS and OCxNOIS bits in TMRx_CTRL2 register
- OCxOIS=0 amd OCxNOIS=0: When idle (MOEN=0), the output level after the dead-time is 0
- OCxOIS=1 amd OCxNOIS=1: When idle (MOEN=0), the output level after the dead-time is 1

（4） RMOS bit in TMRx_BDT register
- Application environment of RMOS: In corresponding complementary channel and timer run mode (MOEN=1), the timer is not working (CCxEN=0, CCxNEN=0) or is working (CCxEN=1, CCxNEN=1)

（5） IMOS bit in TMRx_BDT register

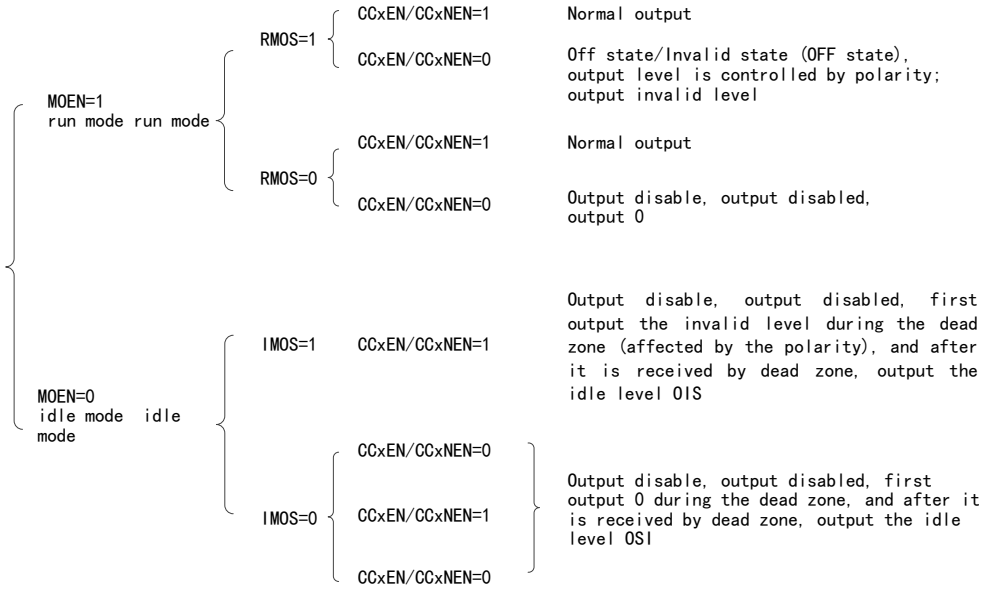
- Application environment of IMOS: In corresponding complementary channel and timer are in idle mode (MOEN=0), the timer is not working (CCxEN=0, CCxNEN=0) or is working (CCxEN=1, CCxNEN=1)

（6） CCxPOL and CCxNPOL bits of TMRx_CCEN register

- CCxPOL=0 and CCxNPOL=0: Output polarity, high level is valid
  CCxPOL=1 and CCxNPOL=1: Output polarity, the low level is valid

The following figure lists the register structure relationships that affect the output waveform

Figure 72 Register Structural Relationship Affecting Output Waveform

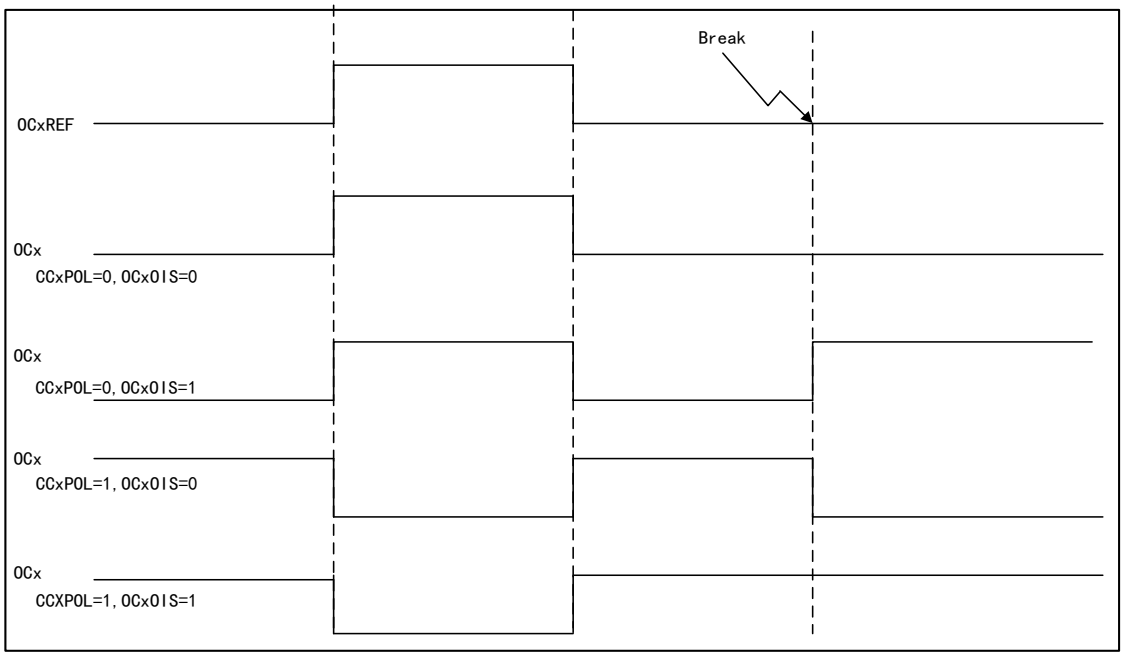


16.4.9 Breaking Function

The signal source of breaking is clock fault event and external input interface. Besides, the BRKEN bit in TMRx_BDT register can enable the breaking function, and the BRKPOL bit can configure the polarity of breaking input signal.

When a breaking event occurs, the output pulse signal level can be modified according to the state of the relevant control bit.

Figure 73 Breaking Event Timing Diagram

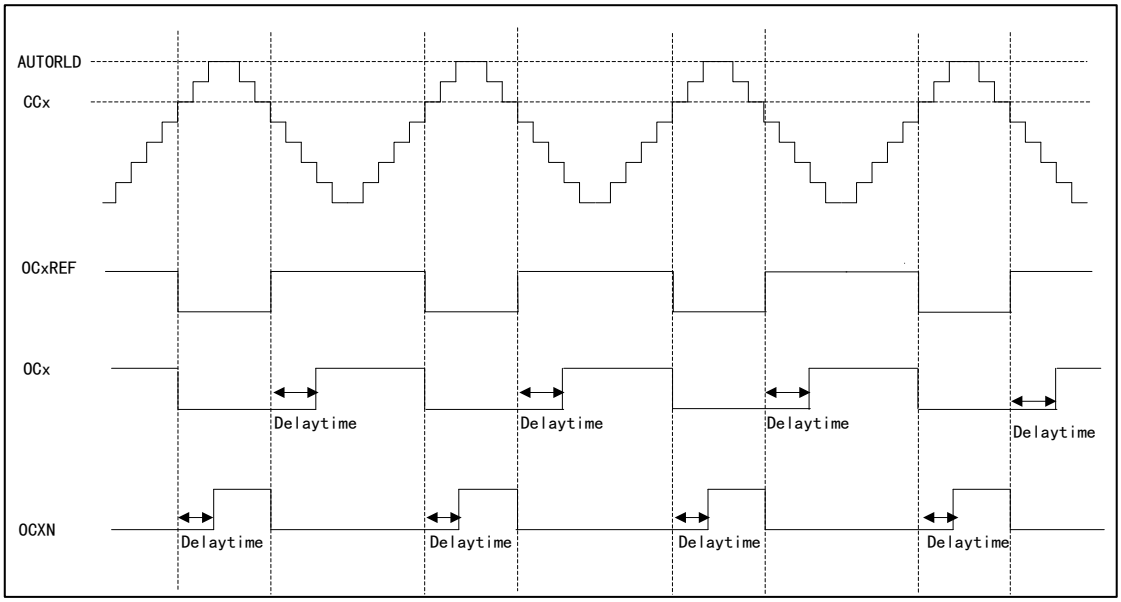


16.4.10 Complementary Output and Dead-time Insertion

Timers 15/16/17 have three groups of complementary ouptut channels. The insertion dead time is used to generate complementary output signals to ensure that the two-way complementary signals of channels will not be valid at the same time. The dead time is set according to the output device connected to the timer and its characteristics

The duration of the dead-time can be controlled by configuring DTS bit of TMRx_BDT register

Figure 74 Complementary Output of Insertion with Dead-time



16.4.11 Forced Output Mode

In the forced output mode, the compare result is ignored, and the corresponding level is directly output according to the configuration instruction.

- CCxSEL=00 for TMRx_CCMx register, set CCx channel as output
- OCxMOD=100/101 for TMRx_CCMx register, set to force OCxREF signal to invalid/valid state

In this mode, the corresponding interrupt and DMA request will still be generated.

16.4.12 Slave Mode (only applicable to TMR15)

TMRx timer can synchronize external trigger

- Reset mode
- Gated mode
- Trigger mode

SMFSEL bit in TMRx_SMCTRL register can be set to select the mode

SMFSEL=100 set the reset mode, SMFSEL=101 set the gated mode, SMFSEL=110 set the trigger mode.

In the reset mode, when a trigger input event occurs, the counter and prescaler will be initialized, and the rising edge of the selected trigger input (TRGI) will reinitialize the counter and generate a signal to update the register.

In the gated mode, the enable of the counter depends on the high level of the selected input. When the trigger input is high, the clock of the counter will be started. Once the trigger input becomes low, the counter will stop (but not be reset). The start and stop of the counter are controlled.

In the trigger mode, the enable of the counter depends on the event on the selected input, the counter is started (but is not reset) at the rising edge of the trigger input, and only the start of the counter is controlled.

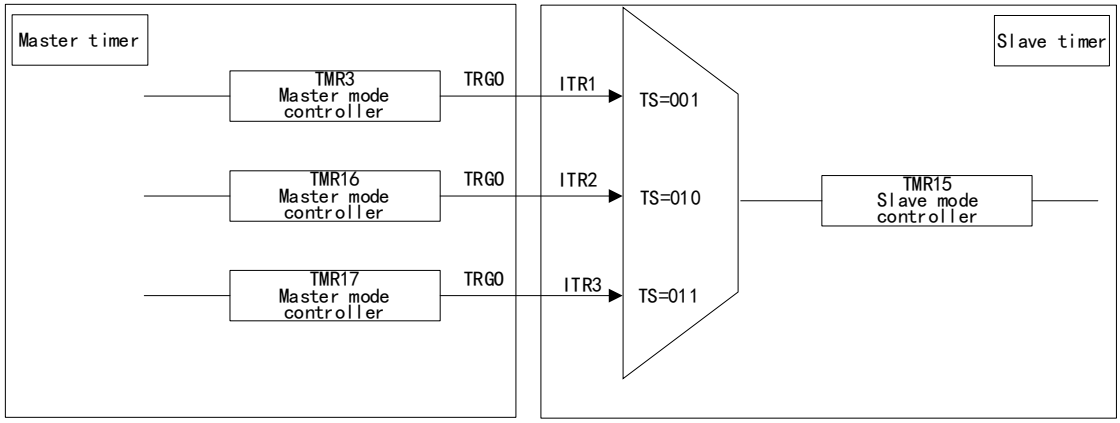
16.4.13 Timer Interconnection (only applicable to TMR15)

This function applies only to APM32E030x8.

Each timer of TMRx can be connected with each other to realize synchronization or cascading between timers. It is required to configure one timer in master mode and the other timer in slave mode.

When the timer is in master mode, it can reset, start, stop and provide clock source for the counter of the slave mode timer.

Figure 75 Interconnection of TMR15 and Other Timers



Note: The trigger signal for the TMR16,TMR17 internal connection is TMR16_CH1,TMR17_CH1.

When the timers are interconnected:

- A timer can be used as the prescaler of other register
- Another register can be started by the enable signal of a timer
- Another register can be started by the update event of a timer
- Another register can be selected by the enable of a timer
- Two timers can be synchronized by an external trigger

16.4.14 Interrupt and DMA Request

The timer can generate an interrupt when an event occurs during operation (TMR15)

- Update event (counter overrun/underrun, counter initialization)
- Trigger event (counter start, stop, internal/external trigger)
- Capture/Compare event
- Breaking signal input event.

The timer can generate an interrupt when an event occurs during operation (TMR16/17)

- Update event (counter overrun)
- Capture/Compare event
- Breaking signal input event.

Some internal interrupt events can generate DMA requests, and special interfaces can enable or disable DMA requests.

16.5 TMR15 Register Address Mapping

In the following table, all registers of TMR15 are mapped to a 16-bit addressable (address) space.

Table 51 TMR15 Register Address Mapping

Register name	Description	Offset address
TMR15_CTRL1	Control register 1	0x00
TMR15_CTRL2	Control register 2	0x04
TMR15_SMCTRL	Slave mode control register	0x08
TMR15_DIEN	DMA/Interrupt enable register	0x0C
TMR15_STS	State register	0x10
TMR15_CEG	Control event generation register	0x14
TMR15_CCM1	Capture/Compare mode register	0x18
TMR15_CCEN	Capture/Compare enable register	0x20
TMR15_CNT	Counter register	0x24
TMR15_PSC	Prescaler register	0x28
TMR15_AUTORLD	Auto reload register	0x2C
TMR15_REPCNT	Repeat count register	0x30
TMR15_CC1	Channel 1 capture/compare register	0x34
TMR15_CC2	Channel 2 capture/compare register	0x38
TMR15_BDT	Break and dead-time register	0x44
TMR15_DCTRL	DMA control register	0x48
TMR15_DMADDR	DMA address register of continuous mode	0x4C

16.6 TMR15 Register Functional Description

16.6.1 Control register 1 (TMR15_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.
1	UD	R/W	Update Disable Update event can cause AUTORLD, PSC and CCx to generate the value of update setting. 0: Update event is allowed (UEV) An update event can occur in any of the following situations: The counter overruns; Set UEG bit; Update generated by slave mode controller. 1: Update event is disabled
2	URSSEL	R/W	Update Request Source Select

Field	Name	R/W	Description
			If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit. 0: The counter overruns; Set UEG bit; Update generated by slave mode controller; 1: The counter overruns
3	SPMEN	R/W	Single Pulse Mode Enable When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed. 0: Disable 1: Enable
6:4	Reserved		
7	ARPEN	R/W	Auto-reload Preload Enable When the buffer is disabled, the program modification TMR15_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMR15_AUTORLD will modify the values loaded to the counter in the next update event. 0: Disable 1: Enable
9:8	CLKDIV	R/W	Clock Divide Factor For the configuration of dead time and digital filter, CK_INT provides the clock, and the dead time and the clock of the digital filter can be adjusted by setting this bit. 00：$t_{DTS}=t_{CK\_INT}$ 01：$t_{DTS}=2\times t_{CK\_INT}$ 10：$t_{DTS}=4\times t_{CK\_INT}$ 11: Reserved
15:10	Reserved		

16.6.2 Control register 2 (TMR15_CTRL2)

Offset address: 0x04

Reset value: 0x0000

Field	Name	R/W	Description
0	CCPEN	R/W	Capture/Compare Preloaded Enable This bit affects the change of CCxEN, CCxNEN and OCxMOD values. When preloading is disabled, the program modification will immediately affect the timer setting; When preloading is enabled, it is only updated after COMG is set, so as to affect the setting of timer; this bit only works on channels with complementary output. 0: Disable 1: Enable
1	Reserved		
2	CCUSEL	R/W	Capture/compare Control Update Select Only when the capture/compare preload is enabled (CCPEN=1), it works only for complementary output channel. 0: It can only be updated by setting COMG bit 1: It can be updated by setting COMG bit or rising edge on TRGI
3	CCDSEL	R/W	Capture/compare DMA Select 0: Send DMA request of CCx when CCx event occurs 1: Send DMA request of CCx when an update event occurs

Field	Name	R/W	Description
6:4	MMSEL	R/W	Master Mode Signal Select The signals of timers working in master mode can be used for TRGO, which affects the work of timers in slave mode and cascaded with master timer, and specifically affects the configuration of timers in slave mode. 000: Reset; the reset signal of master mode timer is used for TRGO 001: Enable; the counter enable signal of master mode timer is used for TRGO 010: Update; the update event of master mode timer is used for TRGO 011: Compare pulses; when the master mode timer captures/compares successfully (CCxIFLG=1), a pulse signal is output for TRGO 100: Compare mode 1; OC1REF is used to trigger TRGO 101: Compare mode 2; OC2REF is used to trigger TRGO 110: Reserved 111: Reserved
7	Reserved		
8	OC1OIS	R/W	OC1 Output Idle State Configure Only the level state after the dead time of OC1 is affected when MOEN=0 and OC1N is realized. 0：OC1=0 1：OC1=1 Note: When LOCKCFG bit in TMRx_BDT register is at the Level 1, 2 or 3, this bit cannot be modified.
9	OC1NOIS	R/W	OC1N Output Idle State Configure Only the level state after the dead time of OC1 is affected when MOEN=0 and OC1N is realized. 0：OC1N=0 1：OC1N=1 Note: When LOCKCFG bit in TMRx_BDT register is at the Level 1, 2 or 3, this bit cannot be modified.
10	OC2OIS	R/W	OC2 Output Idel State Configure Refer to the description of OC1OIS bit
15:11	Reserved		

16.6.3 Slave mode control register (TMR15_SMCTRL)

Offset address: 0x08

Reset value: 0x0000

Field	Name	R/W	Description
2:0	SMFSEL	R/W	Slave Mode Function Select 000: Disable the slave mode, the timer can be used as master mode timer to affect the work of slave mode timer; if CTRL1_CNTEN=1, the prescaler is directly driven by the internal clock. 001: Encoder mode 1; according to the level of TI1FP1, the counter counts at the edge of TI2FP2. 010: Encoder mode 2; according to the level of TI2FP2, the counter counts at the edge of TI1FP1. 011: Encoder mode 3; according to the input level of another signal, the counter counts at the edge of TI1FP1 and TI2FP2. 100: Reset mode; the slave mode timer resets the counter after receiving the rising edge signal of TRGI and generates the signal to update the register. 101: Gated mode; the slave mode timer starts the counter to work after receiving the TRGI high level signal; it stops the counter when receiving TRGI low level; when receiving TRGI high level signal again, the timer will continue to work; the counter is not reset during the whole period.

Field	Name	R/W	Description
			110: Trigger mode, the slave mode timer starts the counter to work after receiving the rising edge signal of TRGI. 111: External clock mode 1; select the rising edge signal of TRGI as the clock source to drive the counter to work.
3	Reserved		
6:4	TRGSEL	R/W	Trigger Input Signal Select In order to avoid false edge detection when changing the bit value, it must be changed when SMFSEL=0. 000: Internal trigger ITR0 001: Internal trigger ITR1 010: Internal trigger ITR2 011: Internal trigger ITR3 100: Channel 1 input edge detector TIF_ED 101: Channel 1 post-filtering timer input TI1FP1 110: Channel 2 post-filtering timer input TI2FP2 111: External trigger input (ETRF)
7	MSMEN	R/W	Master/slave Mode Enable 0: Invalid 1: Enable the master/slave mode
15:8	Reserved		

Table 52 TMR15 Internal Trigger Connection

Slave timer	ITR1（TS=000）	ITR2（TS=010）	ITR3（TS=011）
TMR15	TMR3	TMR16	TMR17

16.6.4 DMA/Interrupt enable register (TMR15_DIEN)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
0	UIEN	R/W	Update interrupt Enable 0: Disable 1: Enable
1	CC1IEN	R/W	Capture/Compare Channel1 Interrupt Enable 0: Disable 1: Enable
2	CC2IEN	R/W	Capture/Compare Channel2 Interrupt Enable 0: Disable 1: Enable
4:3	Reserved		
5	COMIEN	R/W	COM Interrupt Enable 0: Disable 1: Enable
6	TRGIEN	R/W	Trigger interrupt Enable 0: Disable 1: Enable
7	BRKIEN	R/W	Break interrupt Enable （1）0: Disable （2）1: Enable
8	UDIEN	R/W	Update DMA Request Enable 0: Disable 1: Enable
9	CC1DEN	R/W	Capture/Compare Channel1 DMA Request Enable 0: Disable

Field	Name	R/W	Description
			1: Enable
10	CC2DEN	R/W	Capture/Compare Channel2 DMA Request Enable 0: Disable 1: Enable
13:11	Reserved		
14	TRGDEN	R/W	Trigger DMA Request Enable 0: Disable 1: Enable
15	Reserved		

16.6.5 State register (TMR15_STS)

Offset address: 0x10

Reset value: 0x0000

Field	Name	R/W	Description
0	UIFLG	RC_W0	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur 1: Update event interrupt occurs When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations: (1) UD=0 on TMRx_CTRL1 register, and when the value of the repeat counter overruns/underruns, an update event will be generated; (2) URSSEL=0 and UD=0 on TMRx_CTRL1 register, configure UEG = 1 on TMR15_CEG register to generate update event, and the counter needs to be initialized by software; (3) URSSEL=0 and UD=0 on TMRx_CTRL1 register, generate update event when the counter is initialized by trigger event.
1	CC1IFLG	RC_W0	Capture/Compare Channel1 Interrupt Flag **When the capture/compare channel 1 is configured as output:** 0: No matching occurred 1: The value of TMR15_CNT matches the value of TMR15_CC1 **When the capture/compare channel 1 is configured as input:** 0: Input capture did not occur 1: Input capture occurred It is set to 1 by hardware when capture event occurs, and can be cleared by software or by reading TMR15_CC1 register.
2	CC2IFLG	RC_W0	Capture/Compare Channel2 i Interrupt Flag Refer to the description of CC1IFLG
4:3	Reserved		
5	COMIFLG	RC_W0	COM Event Interrupt Generate Flag 0: COM event does not occur 1: COM interrupt waits for response After COM event is generated, this bit is set to 1 by hardware and cleared by software.
6	TRGIFLG	RC_W0	Trigger Event Interrupt Generate Flag 0: Trigger event interrupt did not occur 1: Trigger event interrupt occurred After Trigger event is generated, this bit is set to 1 by hardware and cleared by software.

Field	Name	R/W	Description
7	BRKIFLG	RC_W0	Break Event Interrupt Generate Flag Bit 0: Break event does not occur 1: Break event occurs When break input is valid, this bit is set to 1 by hardware; when break input is invalid, this bit can be cleared by software.
8	Reserved		
9	CC1RCFLG	RC_W0	Capture/compare Channel1 Repetition Capture Flag 0: Repeat capture does not occur 1: Repeat capture occurs The value of the counter is captured in TMR15_CC1 register, and CC1IFLG=1; only when the channel is configured as input capture, can this bit be set to 1 by hardware and cleared by software.
10	CC2RCFLG	RC_W0	Capture/compare Channel2 Repetition Capture Flag Refer to the description of CC1RCFLG.
15:11	Reserved		

16.6.6 Control event generation register (TMR15_CEG)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared by hardware. Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMRx_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared.
1	CC1EG	W	Capture/Compare Channel1 Event Generation 0: Invalid 1: Capture/Compare event is generated This bit is set to 1 by software and cleared automatically by hardware. If Channel 1 is in output mode, When CC1IFLG=1, if CC1IEN and CC1DEN bits are set, the corresponding interrupt and DMA request will be generated. If Channel 1 is in input mode The value of the capture counter is stored in TMR15_CC1 register; configure CC1IFLG=1, and if CC1IEN and CC1DEN bits are also set, the corresponding interrupt and DMA request will be generated; at this time, if CC1IFLG=1, it is required to configure CC1RCFLG=1.
2	CC2EG	W	Capture/Compare Channel2 Event Generation Refer to CC1EG description
4:3	Reserved		
5	COMG	W	Capture/Compare Control Update Event Generate 0: Invalid 1: Capture/Compare update event is generated This bit is set to 1 by software and cleared automatically by hardware. Note: COMG bit is valid only in complementary output channel.
6	TEG	W	Trigger Event Generate 0: Invalid 1: Trigger event is generated

Field	Name	R/W	Description
			This bit is set to 1 by software and cleared automatically by hardware.
7	BEG	W	Break Event Generate 0: Invalid 1: Break event is generated This bit is set to 1 by software and cleared automatically by hardware.
15:8	Reserved		

16.6.7 Capture/Compare mode register (TMR15_CCM1)

Offset address: 0x18

Reset value: 0x0000

The timer can be configured as input (capture mode) or output (compare mode) by CCxSEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output mode and input mode. The OCxx in the register describes the function of the channel in the output mode, and the ICxx in the register describes the function of the channel in the input mode.

Output compare mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select This bit defines the input/output direction and the selected input pin. 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR15_CCEN register CC1EN=0).
2	OC1FEN	R/W	Output Compare Channel1 Fast Enable 0: Disable 1: Enable This bit is used to improve the response of the capture/compare output to the trigger input event.
3	OC1PEN	R/W	Output Compare Channel1 Preload Enable 0: Preloading function is disabled; write the value of TMRx_CC1 register through the program and it will work immediately. 1: Preloading function is enabled; write the value of TMRx_CC1 register through the program and it will work after an update event is generated. Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain.
6:4	OC1MOD	R/W	Output Compare Channel1 Mode Configure 000: Freeze The output compare has no effect on OC1REF 001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture/compare register, OC1REF will be forced to be at high level 010: The output value is low when matching. When the value of the counter matches the value of the capture/compareregister, OC1REF will be forced to be at low level

Field	Name	R/W	Description
			011: Output flaps when matching. When the value of the counter matches the value of the capture/registerregister, flap the level of OC1REF 100: The output is forced to be ow Force OC1REF to be at low level 101: The output is forced to be high. Force OC1REF to be at high level 110: PWM mode 1 (set to high when the counter value<output compare value; otherwise, set to low) 111: PWM mode 2 (set to high when the counter value>output compare value; otherwise, set to low) Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the compare result changes or when the output compare mode changes from freeze mode to PWM mode.
7	Reserved		
9:8	CC2SEL	R/W	Capture/Compare Channel2 Select This bit defines the input/output direction and the selected input pin. 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI2 10: CC2 channel is input, and IC2 is mapped on TI1 11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR15_CCEN register CC2EN=0).
10	OC2FEN	R/W	Output Compare Channel2 Preload Enable Refer to the description of OC1FEN.
11	OC2PEN	R/W	Output Compare Channel2 Buffer Enable Refer to the description of OC1PEN.
14:12	OC2MOD	R/W	Output Compare Channel1 Mode Refer to the description of OC1MOD.
15	Reserved		

Input capture mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 10: CC1 channel is input, and IC1 is mapped on TI2 11: CC1 channel is input, and IC1 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR15_CCEN bit CC1EN=0).
3:2	IC1PSC	R/W	Input Capture Channel 1 Perscaler Configure 00：PSC=1 01：PSC=2 10：PSC=4 11：PSC=8 PSC is prescaled factor, which triggers capture once every PSC events.
7:4	IC1F	R/W	Input Capture Channel 1 Filter Configure 0000: Filter disabled, sampling by f_{DTS} 0001：DIV=1，N=2 0010：DIV=1，N=4 0011：DIV=1，N=8 0100：DIV=2，N=6 0101：DIV=2，N=8

Field	Name	R/W	Description
			0110：DIV=4，N=6 0111：DIV=4，N=8 1000：DIV=8，N=6 1001：DIV=8，N=8 1010：DIV=16，N=5 1011：DIV=16，N=6 1100：DIV=16，N=8 1101：DIV=32，N=5 1110：DIV=32，N=6 1111：DIV=32，N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events.
9:8	CC2SEL	R/W	Capture/Compare Channel 2 Select 00: CC2 channel is output 01: CC2 channel is input, and IC2 is mapped on TI2 10: CC2 channel is input, and IC2 is mapped on TI1 11: CC2 channel is input, and IC2 is mapped on TRC, and only works in internal trigger input Note: This bit can be written only when the channel is disabled (TMR15_CCEN register CC2EN=0).
11:10	IC2PSC	R/W	Input Capture Channel 2 Perscaler Configure Refer to the description of IC1PSC.
15:12	IC2F	R/W	Input Capture Channel 2 Filter Configure Refer to the description of IC1F.

16.6.8 Capture/Compare enable register (TMR15_CCEN)

Offset address: 0x20

Reset value: 0x0000

Field	Name	R/W	Description
0	CC1EN	R/W	Capture/Compare Channel1 Output Enable **When the capture/compare channel 1 is configured as output:** 0: Output is disabled 1: Output is enabled **When the capture/compare channel 1 is configured as input:** This bit determines whether the value CNT of the counter can be captured and enter TMR15_CC1 register 0: Capture is disabled 1: Capture is enabled
1	CC1POL	R/W	Capture/Compare Channel1 Output Polarity Configure When CC1 channel is configured as output: 0: OC1 high level is valid 1: OC1 low level is valid When CC1 channel is configured as input: CC1POL and CC1NPOL control the polarity of the triggered or captured signals TI1FP1 and TI2FP1 at the same time 00: Non-phase-inverting/rising edge: TIxFP1 is not reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode). 01: Inverted phase/Falling edge:

Field	Name	R/W	Description
			TIxFP1 is reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode). 10: Reserved 11: Non-phase-inverting/Rising and falling edges: TIxFP1 is not reversed phase (triggered in gated mode, cannot be used in encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode).
2	CC1NEN	R/W	Capture/Compare Channel1 Complementary Output Enable 0: Disable 1: Enable
3	CC1NPOL	R/W	Capture/Compare Channel1 Complementary Output Polarity 0: OC1N high level is valid 1: OC1N low level is valid Note: When the protection level is 2 or 3, this bit cannot be modified
4	CC2EN	R/W	Capture/Compare Channel2 Output Enable Refer to the description of CCEN_CC1EN
5	CC2POL	R/W	Capture/Compare Channel2 Output Polarity Configure Refer to the description of CCEN_CC1POL
6	Reserved		
7	CC2NPOL	R/W	Capture/Compare Channel2 Complementary Output Polarity Configure Refer to the description of CCEN_CC1NPOL
15:8	Reserved		

16.6.9 Counter register (TMR15_CNT)

Offset address: 0x24

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CNT	R/W	Counter Value

16.6.10 Prescaler register (TMR15_PSC)

Offset address: 0x28

Reset value: 0x0000

Field	Name	R/W	Description
15:0	PSC	R/W	Prescaler Value Clock frequency of counter (CK_CNT)＝f_{CK_PSC}/(PSC+1).

16.6.11 Auto reload register (TMR15_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF

Field	Name	R/W	Description
15:0	AUTORLD	R/W	Auto Reload Value When the value of auto reload is empty, the counter will not count.

16.6.12 Repeat counter register (TMR15_REPCNT)

Offset address: 0x30

Reset value: 0x0000

Field	Name	R/W	Description
7:0	REPCNT	R/W	Repetition Counter Value When the count value of the repeat counter is reduced to 0, an update event will be generated, and the counter will start counting again from the REPCNT value; the new value newly written to this register is valid only when an update event occurs in next cycle.
15:8	Reserved		

16.6.13 Channel 1 capture/compare register (TMR15_CC1)

Offset address: 0x34

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC1	R/W	Capture/Compare Channel 1 Value **When the capture/compare channel 1 is configured as input mode:** CC1 contains the counter value transmitted by the last input capture channel 1 event. **When the capture/compare channel 1 is configured as output mode:** CC1 contains the current load capture/compare register value Compare the value CC1 of the capture and compare channel 1 with the value CNT of the counter to generate the output signal on OC1. When the output compare preload is disabled (OC1PEN=0 for TMRx_CCM1 register), the written value will immediately affect the output compare results; If the output compare preload is enabled (OC1PEN=1 for TMRx_CCM1 register), the written value will affect the output compare result when an update event is generated.

16.6.14 Channel 2 capture/compare register (TMR15_CC2)

Offset address: 0x38

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC2	R/W	Capture/Compare Channel 2 Value Refer to the description of TMR15_CC1

16.6.15 Break and dead-time register (TMR15_BDT)

Offset address: 0x44

Reset value: 0x0000

According to the lock setting, AOEN, BRKPOL, BRKEN, IMOS, RMOS and DTS[7:0] bits all can be write-protected, and it is necessary to configure them when writing to TMRx_BDT register for the first time.

Field	Name	R/W	Description
7:0	DTS	R/W	Dead Time Setup DT is the dead duration, and the relationship between DT and register DTS is as follows: DTS[7:5]=0xx=>DT=DTS[7:0]×T_{DTS}，T_{DTS}=TDTS； DTS[7:5]=10x=>DT=（64+DTS[5:0])×T_{DTS}，T_{DTS}=2×T_{DTS}； DTS[7:5]=110=>DT=（32+DTS[4:0])×T_{DTS}，T_{DTS}=8×T_{DTS}； DTS[7:5]=111=>DT=（32+DTS[4:0]）×T_{DTS}，T_{DTS}=16×T_{DTS}； For example: assuming T_{DTS} =125ns (8MHZ), the dead time setting is as follows: If the step time is 125ns, the dead time can be set from 0 to 15875ns; If the step time is 250ns, the dead time can be set from 16μs to 31750ns; If the step time is 1μs, the dead time can be set from 32μs to 63μs;

Field	Name	R/W	Description
			If the step time is 2μs, the dead time can be set from 64μs to 126μs. Note: Once LOCK level (LOCKCFG bit in TMR15_BDT register) is set to 1, 2 or 3, these bits cannot be modified.
9:8	LOCKCFG	R/W	Lock Write Protection Mode Configure 00: Without Lock write protection level; the register can be written directly 01: Lock write protection level 1 It cannot be written to DTS, BRKEN, BRKPOL and AOEN bits of TMR15_BDT, and OCxOIS and OCxNOIS bits of TMR15_CTRL2 register. 02: Lock write protection level 2 It is not allowed to write to all bits with protection level 1 and write to the CCxPOL and OCxNPOL bits in TMR15_CCEN register and the RMOS and IMOS bits in TMR15_BDT register. 11: Lock write protection level 3 It is not allowed to write to all bits with protection level 2, and write to the OCxMOD and OCxPEN bits of TMR15_CCMx register. Note: After system reset, the lock write protect bit can only be written once.
10	IMOS	R/W	Idle Mode Off-state Configure Idle mode means MOEN=0; disable means CcxEN=0; this bit describes the impact of different values for this bit on the output waveform when MOEN=0 and CcxEN changes from 0 to 1. 0: OCx/OCxN output is disabled 1: If CCxEN=1, the invalid level is output during the dead time (the specific level value is affected by the polarity configuration), and the idle level is output after the dead time
11	RMOS	R/W	Run Mode Off-state Configure Run mode means MOEN=1; disable means CcxEN=0; this bit describes the impact of different values for this bit on the output waveform when MOEN=1 and CcxEN changes from 0 to 1. 0: OCx/OCxN output is disabled 1: OCx/OCxN first outptus invalid level (the specific level value is affected by the polarity configuration)
12	BRKEN	R/W	Break Function Enable 0: Disable 1: Enable Note: When the protection level is 1, this bit cannot be modified.
13	BRKPOL	R/W	Break Polarity Configure 0: The break input BRK is valid at low level 1: The break input BRK is valid at high level Note: When the protection level is 1, this bit cannot be modified. Writing to this bit requires an APB clock delay before it can be used.
14	AOEN	R/W	Automatic Output Enable 0: MOEN can only be set to 1 by software 1: MOEN can be set to 1 by software or be automatically set to 1 in next update event (breaking input is ineffective) Note: When the protection level is 1, this bit cannot be modified.
15	MOEN	R/W	Wave Main Output Enable 0: Disable the output of OCx and OCxN or force the output of idle state 1: When CCxEN and CCxNEN bits of the TMR15_CCEN register are set, turn on OCx and OCxN output When the break input is valid, it is cleared by hardware asynchronously. Note: Setting to 1 by software or setting to 1 automatically depends on AOEN bit of the TMR15_BDT register.

16.6.16 DMA control register (TMR15_DCTRL)

Offset address: 0x48

Reset value: 0x0000

Field	Name	R/W	Description
4:0	DBADDR	R/W	DMA Base Address Setup These bits define the base address of DMA in continuous mode (when reading or writing TMR15_DMA register), and DBADDR is defined as the offset from the address of TMR15_CTRL1 register: 00000：TMR15_CTRL1 00001：TMR15_CTRL2 00010：TMR15_SMCTRL …….
7:5	Reserved		
12:8	DBLEN	R/W	DMA Burst Transfer Length Setup These bits define the transfer length and transfer times of DMA in continuous mode. The data transferred can be 16 bits and 8 bits. When reading/writing TMRx_DMADDR register, the timer will conduct a continuous transmission; 00000: Transmission for 1 time 00001: Transmission for 2 times 00010: Transmission for 3 times …… 10001: Transmission for 18 times The transmission address formula is as follows: Transmission address=TMRx_CTRL1 address (slave address) +DBADDR+DMA index; DMA index=DBLEN For example: DBLEN=7, DBADDR=TMR1_CTRL1 (slave address) means the address of the data to be transmitted, while the address +DBADDR+7 of TMRx_CTRL1 means the address of the data to be written/read, Data transmission will occur to: TMRx_CTRL1 address + seven registers starting from DBADDR. The data transmission will change according to different DMA data length: When the transmission data is set to 16 bits, the data will be transmitted to seven registers.When the transmission data is set to 8 bits, the data of the first register is the MSB bit of the first data, the data of the second register is the LSB bit of the first data, and the data will still be transmitted to seven registers.
15:13	Reserved		

16.6.17 DMA address register of continuous mode (TMR15_DMADDR)

Offset address: 0x4C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	DMADDR	R/W	DMA Register for Burst Transfer Read or write operation access of TMR15_DMADDR register may lead to access operation of the register in the following address: TMR15_CTRL1 address + (DBADDR+DMA index) ×4 Wherein: "TMR15_CTRL1 address" is the address of control register 1 (TMR15_CTRL1); "DBADDR" is the base address defined in TMR15_DCTRL register; "DMA index" is the offset automatically controlled by DMA, and it depends on DBLEN defined in TMR15_DCTRL register.

16.7 TMR16 and TMR17 Register Address Mapping

In the following table, all registers of TMR16 and TMR17 are mapped to a 16-bit addressable (address) space.

Table 53 TMR16 and TMR17 Register Address Mapping

Register name	Description	Offset address
TMRx_CTRL1	Control register 1	0x00
TMRx_CTRL2	Control register 2	0x04
TMRx_DIEN	DMA/Interrupt enable register	0x0C
TMRx_STS	State register	0x10
TMRx_CEG	Control event generation register	0x14
TMRx_CCM1	Capture/Compare mode register	0x18
TMRx_CCEN	Capture/Compare enable register	0x20
TMRx_CNT	Counter register	0x24
TMRx_PSC	Prescaler register	0x28
TMRx_AUTORLD	Auto reload register	0x2C
TMRx_REPCNT	Repeat count register	0x30
TMRx_CC1	Channel 1 capture/compare register	0x34
TMRx_BDT	Break and dead-time register	0x44
TMRx_DCTRL	DMA control register	0x48
TMRx_DMADDR	DMA address register of continuous mode	0x4C

16.8 TMR16 and TMR17 Register Functional Description

16.8.1 Control register 1 (TMRx_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.
1	UD	R/W	Update Disable Update event can cause AUTORLD, PSC and CCx to generate the value of update setting. 0: Update event is allowed (UEV) An update event can occur in any of the following situations: The counter overruns; Set UEG bit; Update generated by slave mode controller. 1: Update event is disabled
2	URSSEL	R/W	Update Request Source Select If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit. 0: The counter overruns Set UEG bit Update generated by slave mode controller 1: The counter overruns
3	SPMEN	R/W	Single Pulse Mode Enable When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed. 0: Disable 1: Enable
6:4	Reserved		
7	ARPEN	R/W	Auto-reload Preload Enable When the buffer is disabled, the program modification TMRx_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMRx_AUTORLD will modify the values loaded to the counter in the next update event. 0: Disable 1: Enable
9:8	CLKDIV	R/W	Clock Divide Factor For the configuration of dead time and digital filter, CK_INT provides the clock, and the dead time and the clock of the digital filter can be adjusted by setting this bit. 00：$t_{DTS}=t_{CK\_INT}$ 01：$t_{DTS}=2\times t_{CK\_INT}$ 10：$t_{DTS}=4\times t_{CK\_INT}$ 11: Reserved
15:10	Reserved		

16.8.2 Control register 2 (TMRx_CTRL2)

Offset address: 0x04

Reset value: 0x0000

Field	Name	R/W	Description
0	CCPEN	R/W	Capture/Compare Preloaded Enable This bit affects the change of CCxEN, CCxNEN and OCxMOD values. When preloading is disabled, the program modification will immediately affect the timer setting; When preloading is enabled, it is only updated after COMG is set, so as to affect the setting of timer; this bit only works on channels with complementary output. 0: Disable 1: Enable
1	Reserved		
2	CCUSEL	R/W	Capture/compare Control Update Select Only when the capture/compare preload is enabled (CCPEN=1), it works only for complementary output channel. 0: It can only be updated by setting COMG bit 1: It can be updated by setting COMG bit or rising edge on TRGI
3	CCDSEL	R/W	Capture/compare DMA Select 0: Send DMA request of CCx when CCx event occurs 1: Send DMA request of CCx when an update event occurs
7:4	Reserved		
8	OC1OIS	R/W	OC1 Output Idle State Configure Only the level state after the dead time of OC1 is affected when MOEN=0 and OC1N is realized. 0：OC1=0 1：OC1=1 Note: When LOCKCFG bit in TMRx_BDT register is at the Level 1, 2 or 3, this bit cannot be modified.
9	OC1NOIS	R/W	OC1N Output Idle State Configure Only the level state after the dead time of OC1 is affected when MOEN=0 and OC1N is realized. 0：OC1N=0 1：OC1N=1 Note: When LOCKCFG bit in TMRx_BDT register is at the Level 1, 2 or 3, this bit cannot be modified.
15:10	Reserved		

16.8.3 DMA/Interrupt enable register (TMRx_DIEN)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
0	UIEN	R/W	Update interrupt Enable 0: Disable 1: Enable
1	CC1IEN	R/W	Capture/Compare Channel1 Interrupt Enable 0: Disable 1: Enable
4:2	Reserved		
5	COMIEN	R/W	COM Interrupt Enable

Field	Name	R/W	Description
			0: Disable 1: Enable
6	Reserved		
7	BRKIEN	R/W	Break interrupt Enable 0: Disable 1: Enable
8	UDIEN	R/W	Update DMA Request Enable 0: Disable 1: Enable
9	CC1DEN	R/W	Capture/Compare Channel1 DMA Request Enable 0: Disable 1: Enable
15:10	Reserved		

16.8.4 State register (TMRx_STS)

Offset address: 0x10

Reset value: 0x0000

Field	Name	R/W	Description
0	UIFLG	RC_W0	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur 1: Update event interrupt occurs When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations: (1) UD=0 on TMRx_CTRL1 register, and when the value of the repeat counter overruns, an update event will be generated; (2) URSSEL=0 and UD=0 on TMRx_CTRL1 register, configure UEG=1 on TMRx_CEG register to generate update event, and the counter needs to be initialized by software;
1	CC1IFLG	RC_W0	Capture/Compare Channel1 Interrupt Flag **When the capture/compare channel 1 is configured as output:** 0: No matching occurred 1: The value of TMRx_CNT matches the value of TMRx_CC1 **When the capture/compare channel 1 is configured as input:** 0: Input capture did not occur 1: Input capture occurred When capture event occurs, the bit is set to 1 by hardware, and it can be cleared by software or cleared when reading TMRx_CC1 register.
4:2	Reserved		
5	COMIFLG	RC_W0	COM Event Interrupt Generate Flag 0: COM event does not occur 1: COM interrupt waits for response After COM event is generated, this bit is set to 1 by hardware and cleared by software.
6	Reserved		

Field	Name	R/W	Description
7	BRKIFLG	RC_W0	Break Event Interrupt Generate Flag Bit 0: Break event does not occur 1: Break event occurs When break input is valid, this bit is set to 1 by hardware; when break input is invalid, this bit can be cleared by software.
8	Reserved		
9	CC1RCFLG	RC_W0	Capture/compare Channel1 Repetition Capture Flag 0: Repeat capture does not occur 1: Repeat capture occurs The value of the counter is captured to TMRx_CC1 register, and CC1IFLG=1; this bit is set to 1 by hardware and cleared by software only when the channel is configured as input capture.
15:10	Reserved		

16.8.5 Control event generation register (TMRx_CEG)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared by hardware. Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged. In the count-down mode, the counter reads the value of TMRx_AUTORLD; in center-aligned mode or count-up mode, the counter will be cleared.
1	CC1EG	W	Capture/Compare Channel1 Event Generation 0: Invalid 1: Capture/Compare event is generated This bit is set to 1 by software and cleared automatically by hardware. If Channel 1 is in output mode: When CC1IFLG=1, if CC1IEN and CC1DEN bits are set, the corresponding interrupt and DMA request will be generated. If Channel 1 is in input mode: The value of the capture counter is stored in TMRx_CC1 register; configure CC1IFLG=1, and if CC1IEN and CC1DEN bits are also set, the corresponding interrupt and DMA request will be generated; at this time, if CC1IFLG=1, it is required to configure CC1RCFLG=1.
4:2	Reserved		
5	COMG	W	Capture/Compare Control Update Event Generate 0: Invalid 1: Capture/Compare update event is generated This bit is set to 1 by software and cleared automatically by hardware. Note: COMG bit is valid only in complementary output channel.
6	Reserved		
7	BEG	W	Break Event Generate 0: Invalid 1: Break event is generated This bit is set to 1 by software and cleared automatically by hardware.
15:8	Reserved		

16.8.6 Capture/Compare mode register 1 (TMRx_CCM1)

Offset address: 0x18

Reset value: 0x0000

The timer can be configured as input (capture mode) or output (compare mode) by CCxSEL bit. The functions of other bits of the register are different in input and output modes, and the functions of the same bit are different in output mode and input mode. The OCxx in the register describes the function of the channel in the output mode, and the ICxx in the register describes the function of the channel in the input mode.

Output compare mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select This bit defines the input/output direction and the selected input pin. 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 1x: Reserve Note: This bit can be written only when the channel is disabled (TMRx_CCEN register CC1EN=0).
2	OC1FEN	R/W	Output Compare Channel1 Fast Enable 0: Disable 1: Enable This bit is used to improve the response of the capture/compare output to the trigger input event.
3	OC1PEN	R/W	Output Compare Channel1 Preload Enable 0: Preloading function is disabled; write the value of TMRx_CC1 register through the program and it will work immediately. 1: Preloading function is enabled; write the value of TMRx_CC1 register through the program and it will work after an update event is generated. Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. When the preload register is uncertain, PWM mode can be used only in single pulse mode (SPMEN=1); otherwise, the following output compare result is uncertain.
6:4	OC1MOD	R/W	Output Compare Channel1 Mode Configure 000: Freeze The output compare has no effect on OC1REF 001: The output value is high when matching. When the value of counter CNT matches the value CCx of capture/compare register, OC1REF will be forced to be at high level 010: The output value is low when matching. When the value of the counter matches the value of the capture/compareregister, OC1REF will be forced to be at low level 011: Output flaps when matching. When the value of the counter matches the value of the capture/compare register, flap the level of OC1REF 100: The output is forced to be ow Force OC1REF to be at low level 101: The output is forced to be high. Force OC1REF to be at high level 110: PWM mode 1 (set to high when the counter value<output compare value; otherwise, set to low) 111: PWM mode 2 (set to high when the counter value>output compare value; otherwise, set to low) Note: When the protection level is 3 and the channel is configured as output, this bit cannot be modified. In PWM modes 1 and 2, the OC1REF level changes when the compare result changes or when the output compare mode changes from freeze mode to PWM mode.
15:7	Reserved		

Input capture mode:

Field	Name	R/W	Description
1:0	CC1SEL	R/W	Capture/Compare Channel 1 Select 00: CC1 channel is output 01: CC1 channel is input, and IC1 is mapped on TI1 1x: Reserve Note: This bit can be written only when the channel is disabled (TMRx_CCEN bit CC1EN=0).
3:2	IC1PSC	R/W	Input Capture Channel 1 Perscaler Configure 00：PSC=1 01：PSC=2 10：PSC=4 11：PSC=8 PSC is prescaled factor, which triggers capture once every PSC events.
7:4	IC1F	R/W	Input Capture Channel 1 Filter Configure 0000: Filter disabled, sampling by f_{DTS} 0001：DIV=1，N=2 0010：DIV=1，N=4 0011：DIV=1，N=8 0100：DIV=2，N=6 0101：DIV=2，N=8 0110：DIV=4，N=6 0111：DIV=4，N=8 1000：DIV=8，N=6 1001：DIV=8，N=8 1010：DIV=16，N=5 1011：DIV=16，N=6 1100：DIV=16，N=8 1101：DIV=32，N=5 1110：DIV=32，N=6 1111：DIV=32，N=8 Sampling frequency=timer clock frequency/DIV; the filter length=N, indicating that a jump is generated by every N events.
15:8	Reserved		

16.8.7 Capture/Compare enable register (TMRx_CCEN)

Offset address: 0x20

Reset value: 0x0000

Field	Name	R/W	Description
0	CC1EN	R/W	Capture/Compare Channel1 Output Enable **When the capture/compare channel 1 is configured as output:** 0: Output is disabled 1: Output is enabled **When the capture/compare channel 1 is configured as input:** This bit determines whether the value CNT of the counter can be captured and enter TMRx_CC1 register 0: Capture is disabled 1: Capture is enabled
1	CC1POL	R/W	Capture/Compare Channel1 Output Polarity Configure When CC1 channel is configured as output: 0: OC1 high level is valid 1: OC1 low level is valid When CC1 channel is configured as input: CC1POL and CC1NPOL control the polarity of the triggered or captured signals TI1FP1 and TI2FP1 at the same time 00: Non-phase-inverting/rising edge:

Field	Name	R/W	Description
			TIxFP1 is not reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode). 01: Inverted phase/Falling edge: TIxFP1 is reversed phase (triggered in gated and encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode). 10: Reserved 11: Non-phase-inverting/Rising and falling edges: TIxFP1 is not reversed phase (triggered in gated mode, cannot be used in encoder mode), and is captured at the rising edge of TIxFP1 (reset trigger, capture, external clock and trigger mode).
2	CC1NEN	R/W	Capture/Compare Channel1 Complementary Output Enable 0: Disable 1: Enable
3	CC1NPOL	R/W	Complementary output polarity of capture/compare channel 1 (Capture/Compare Channel1 Complementary Output Polarity) 0: OC1N high level is valid 1: OC1N low level is valid Note: When the protection level is 2 or 3, this bit cannot be modified
15:4	Reserved		

16.8.8 Counter register (TMRx_CNT)

Offset address: 0x24

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CNT	R/W	Counter Value

16.8.9 Prescaler register (TMRx_PSC)

Offset address: 0x28

Reset value: 0x0000

Field	Name	R/W	Description
15:0	PSC	R/W	Prescaler Value Clock frequency of counter (CK_CNT)＝f_{CK_PSC}/(PSC+1).

16.8.10 Auto reload register (TMRx_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF

Field	Name	R/W	Description
15:0	AUTORLD	R/W	Auto Reload Value When the value of auto reload is empty, the counter will not count.

16.8.11 Repeat count register (TMRx_REPCNT)

Offset address: 0x30

Reset value: 0x0000

Field	Name	R/W	Description
7:0	REPCNT	R/W	Repeat counter value (Repetition Counter Value When the count value of the repeat counter is reduced to 0, an update event will be generated, and the counter will start counting again from the REPCNT value; the new value newly written to this register is valid only when an update event occurs in next cycle.
15:8	Reserved		

16.8.12 Channel 1 capture/compare register (TMRx_CC1)

Offset address: 0x34

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CC1	R/W	Capture/Compare Channel 1 Value **When the capture/compare channel 1 is configured as input mode:** CC1 contains the counter value transmitted by the last input capture channel 1 event. **When the capture/compare channel 1 is configured as output mode:** CC1 contains the current load capture/compare register value Compare the value CC1 of the capture and compare channel 1 with the value CNT of the counter to generate the output signal on OC1. When the output compare preload is disabled (OC1PEN=0 for TMRx_CCM1 register), the written value will immediately affect the output compare results; If the output compare preload is enabled (OC1PEN=1 for TMRx_CCM1 register), the written value will affect the output compare result when an update event is generated.

16.8.13 Break and dead-time register (TMRx_BDT)

Offset address: 0x44

Reset value: 0x0000

According to the lock setting, AOEN, BRKPOL, BRKEN, IMOS, RMOS and DTS[7:0] bits all can be write-protected, and it is necessary to configure them when writing to TMRx_BDT register for the first time.

Field	Name	R/W	Description
7:0	DTS	R/W	Dead Time Setup DT is the dead duration, and the relationship between DT and register DTS is as follows: DTS[7:5]=0xx=>DT=DTS[7:0]×T_{DTS}，T_{DTS}=T_{DTS}； DTS[7:5]=10x=>DT=（64+DTS[5:0])×T_{DTS}，T_{DTS}=2×T_{DTS}； DTS[7:5]=110=>DT=（32+DTS[4:0])×T_{DTS}，T_{DTS}=8×T_{DTS}； DTS[7:5]=111=>DT=（32+DTS[4:0]）×T_{DTS}，T_{DTS}=16×T_{DTS}； For example: assuming T_{DTS} =125ns (8MHZ), the dead time setting is as follows: If the step time is 125ns, the dead time can be set from 0 to 15875ns; If the step time is 250ns, the dead time can be set from 16μs to 31750ns; If the step time is 1μs, the dead time can be set from 32μs to 63μs; If the step time is 2μs, the dead time can be set from 64μs to 126μs. Note: Once LOCK level (LOCKCFG bit in TMRx_BDT register) is set to 1, 2 or 3, these bits cannot be modified.
9:8	LOCKCFG	R/W	Lock Write Protection Mode Configure 00: Without Lock write protection level; the register can be written directly 01: Lock write protection level 1

Field	Name	R/W	Description
			It cannot be written to DTS, BRKEN, BRKPOL and AOEN bits of TMRx_BDT, and OCxOIS and OCxNOIS bits of TMRx_CTRL2 register. 10: Lock write protection level 2 It is not allowed to write to all bits with protection level 1 and write to the CCxPOL and OCxNPOL bits in TMRx_CCEN register and the RMOS and IMOS bits in TMRx_BDT register. 11: Lock write protection level 3 It is not allowed to write to all bits with protection level 2, and write to the OCxMOD and OCxPEN bits of TMRx_CCMx register. Note: After system reset, the lock write protect bit can only be written once.
10	IMOS	R/W	Idle Mode Off-state Configure Idle mode means MOEN=0; disable means CcxEN=0; this bit describes the impact of different values for this bit on the output waveform when MOEN=0 and CcxEN changes from 0 to 1. 0: OCx/OCxN output is disabled 1: If CCxEN=1, the invalid level is output during the dead time (the specific level value is affected by the polarity configuration), and the idle level is output after the dead time
11	RMOS	R/W	Run Mode Off-state Configure Run mode means MOEN=1; disable means CcxEN=0; this bit describes the impact of different values for this bit on the output waveform when MOEN=1 and CcxEN changes from 0 to 1. 0: OCx/OCxN output is disabled 1: OCx/OCxN first outptus invalid level (the specific level value is affected by the polarity configuration)
12	BRKEN	R/W	Break Function Enable 0: Disable 1: Enable Note: When the protection level is 1, this bit cannot be modified.
13	BRKPOL	R/W	Break Polarity Configure 0: The break input BRK is valid at low level 1: The break input BRK is valid at high level Note: When the protection level is 1, this bit cannot be modified. Writing to this bit requires an APB clock delay before it can be used.
14	AOEN	R/W	Automatic Output Enable 0: MOEN can only be set to 1 by software 1: MOEN can be set to 1 by software or be automatically set to 1 in next update event (breaking input is ineffective) Note: When the protection level is 1, this bit cannot be modified.
15	MOEN	R/W	PWM Main Output Enable 0: Disable the output of OCx and OCxN or force the output of idle state 1: When CCxEN and CCxNEN bits of the TMRx_CCEN register are set, turn on OCx and OCxN output When the break input is valid, it is cleared by hardware asynchronously. Note: Setting to 1 by software or setting to 1 automatically depends on AOEN bit of the TMRx_BDT register.

16.8.14 DMA control software (TMRx_DCTRL)

Offset address: 0x48

Reset value: 0x0000

Field	Name	R/W	Description
4:0	DBADDR	R/W	DMA Base Address Setup These bits define the base address of DMA in continuous mode (when reading or writing TMRx_DMADDR register), and DBADDR is defined as the offset from the address of TMRx_CTRL1 register: 00000：TMRx_CTRL1 00001：TMRx_CTRL2

Field	Name	R/W	Description
			00010：TMRx_SMCTRL …….
7:5	Reserved		
12:8	DBLEN	R/W	DMA Burst Transfer Length Setup These bits define the transfer length and transfer times of DMA in continuous mode. The data transferred can be 16 bits and 8 bits. When reading/writing TMRx_DMADDR register, the timer will conduct a continuous transmission; 00000: Transmission for 1 time 00001: Transmission for 2 times 00010: Transmission for 3 times …… 10001: Transmission for 18 times The transmission address formula is as follows: Transmission address=TMRx_CTRL1 address (slave address) +DBADDR+DMA index; DMA index=DBLEN For example: DBLEN=7, DBADDR=TMR1_CTRL1 (slave address) means the address of the data to be transmitted, while the address +DBADDR+7 of TMRx_CTRL1 means the address of the data to be written/read, Data transmission will occur to: TMRx_CTRL1 address + seven registers starting from DBADDR. The data transmission will change according to different DMA data length: When the transmission data is set to 16 bits, the data will be transmitted to seven registers; When the transmission data is set to 8 bits, the data of the first register is the MSB bit of the first data, the data of the second register is the LSB bit of the first data, and the data will still be transmitted to seven registers.
15:13	Reserved		

16.8.15 DMA address register of continuous mode (TMRx_DMADDR)

Offset address: 0x4C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	DMADDR	R/W	DMA Register for Burst Transfer Read or write operation access of TMRx_DMADDR register may lead to access operation of the register in the following address: TMRx_CTRL1 address + (DBADDR+DMA index) ×4 Wherein: "TMRx_CTRL1 address" is the address of control register 1 (TMRx_CTRL1); "DBADDR" is the base address defined in TMRx_DCTRL register; "DMA index" is the offset automatically controlled by DMA, and it depends on DBLEN defined in TMRx_DCTRL register.

17 Basic Timer (TMR6)

17.1 Introduction

The basic timers TMR6 have an unsigned 16-bit counter, auto reload register, prescaler and trigger controller.

The basic timer provides time reference for general-purpose timer, and can generate DMA request by configuration.

17.2 Main Characteristics

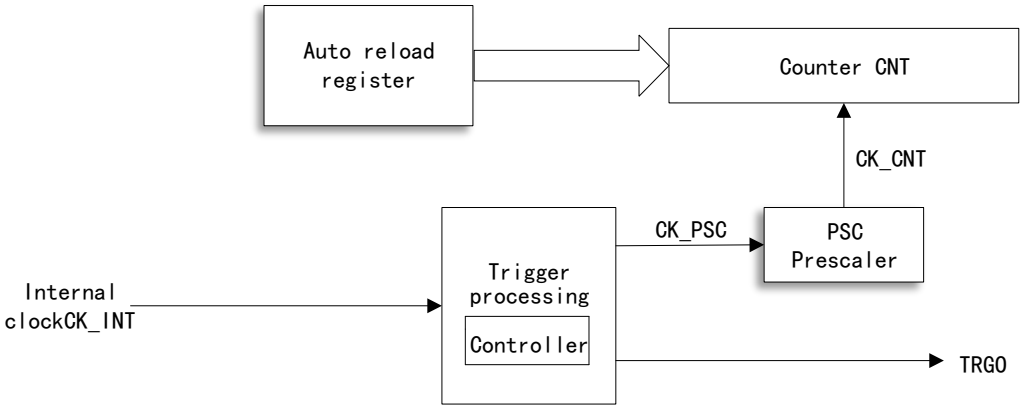
（1） Counter: 16-bit counter, which can only count up

（2） Prescaler: 16-bit programmable prescaler

（3） Clock source: There is only internal clock

17.3 Structure Block Diagram

Figure 76 Basic Timer Structure Block Diagram



17.4 Functional Description

17.4.1 Clock source Selection

The basic timer is driven by internal clock source TMR6_CLK

Configure the CNTEN bit of TMR6_CTRL1 register to enable the counter; when CNTEN bit is set, the internal clock CK_INT can generate CK_INT to drive the counter through the controller and prescaler.

17.4.2 Timebase Unit

The time base unit in the basic timer contains three registers:

- Counter register (CNT) 16 bits
- Auto reload register (AUTORLD) 16 bits
- Prescaler register (PSC) 16 bits

Counter CNT

The basic timer only has one count mode: count-up

Count-up mode

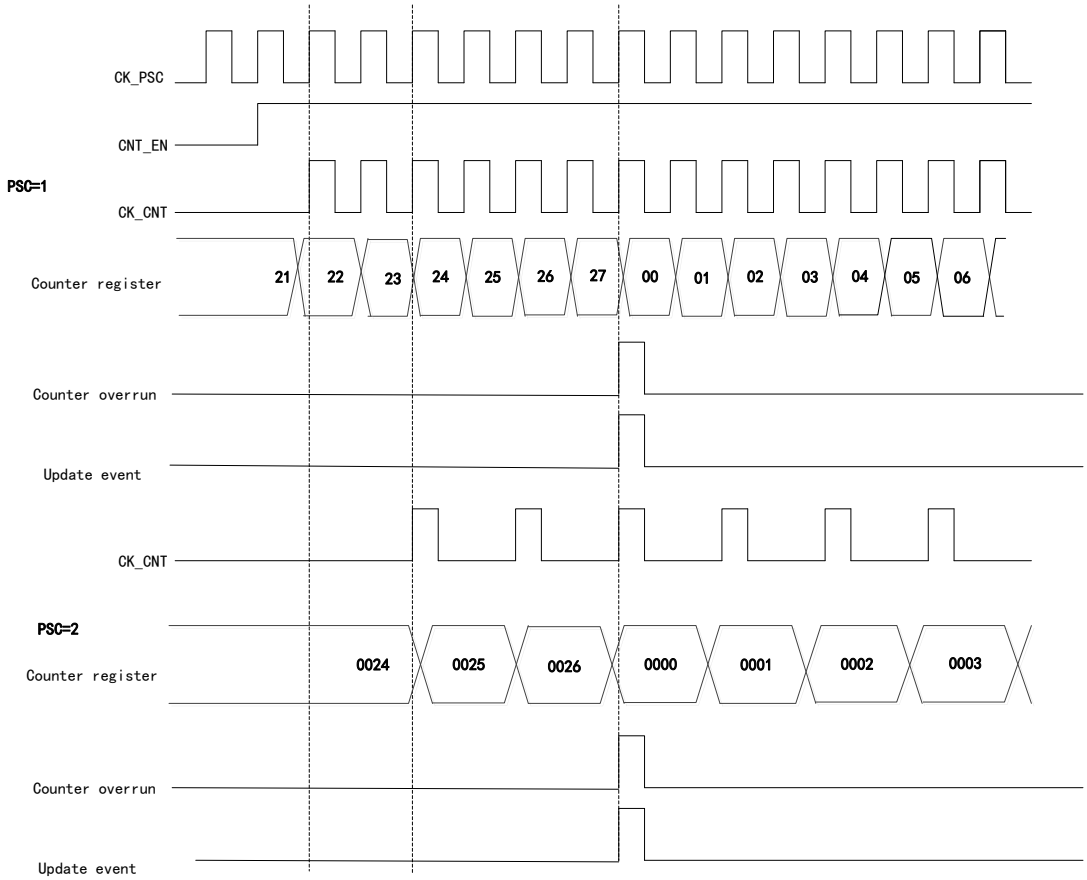
When the counter is in count-up mode, the counter will count up from 0; every

time a pulse is generated, the counter will increase by 1 and when the value of the counter (TMR6_CNT) is equal to the value of the auto reload (TMR6_AUTORLD), then the counter will start to count again from 0, a count-up overrun event will be generated, and the value of the auto reload (TMR6_AUTORLD) is written in advance.

Disable the update event and set UD bit of TMR6_CTRL1 register to 1.

When an update event occurs, both the auto reload register and the prescaler register will be updated.

Figure 77 Counter Timing Diagram, the internal clock division factor is 1 or 2



Prescaler PSC

The prescaler is 16 bits and programmable, and it can divide the clock frequency of the counter to any value between 1 and 65536 (controlled by TMR6_PSC register), and after frequency division, the clock will drive the counter CNT to count. The prescaler has a buffer, which can be changed during running.

17.5 Register Address Mapping

In the following table, all registers of TMR6/TMR7 are mapped to a 16-bit addressable (address) space.

Table 54 TMR6 and TMR7 Register Address Mapping

Register name	Description	Offset address
TMR6_CTRL1	Control register 1	0x00
TMR6_DIEN	DMA/Interrupt enable register	0x0C
TMR6_STS	State register	0x10
TMR6_CEG	Control event generation register	0x14
TMR6_CNT	Counter register	0x24
TMR6_PSC	Prescaler register	0x28
TMR6_AUTORLD	Auto reload register	0x2C

17.6 Register Functional Description

17.6.1 Control register 1 (TMR6_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	CNTEN	R/W	Counter Enable 0: Disable 1: Enable When the timer is configured as external clock, gated mode and encoder mode, it is required to write 1 to the bit by software to start regular work; when it is configured as the trigger mode, it can be written to 1 by hardware.
1	UD	R/W	Update Disable Update event can cause AUTORLD, PSC and CCx to generate the value of update setting. 0: Update event is allowed (UEV) An update event can occur in any of the following situations: The counter overruns/underruns; Set UEG bit; Update generated by slave mode controller. 1: Update event is disabled
2	URSSEL	R/W	Update Request Source Select If interrupt or DMA is enabled, the update event can generate update interrupt or DMA request. Different update request sources can be selected through this bit. 0: The counter overruns or underruns Set UEG bit Update generated by slave mode controller 1: The counter overruns
3	SPMEN	R/W	Single Pulse Mode Enable When an update event is generated, the output level of the channel can be changed; in this mode, the CNTEN bit will be cleared, the counter will be stopped, and the output level of the channel will not be changed. 0: Disable 1: Enable
6:4	Reserved		
7	ARPEN	R/W	Auto-reload Preload Enable

Field	Name	R/W	Description
			When the buffer is disabled, the program modification TMR6_AUTORLD will immediately modify the values loaded to the counter; when the buffer is enabled, the program modification TMR6_AUTORLD will modify the values loaded to the counter in the next update event. 0: Disable 1: Enable
15:8	Reserved		

17.6.2 DMA/Interrupt enable register (TMR6_DIEN)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
0	UIEN	R/W	Update interrupt Enable 0: Disable 1: Enable
7:1	Reserved		
8	UDIEN	R/W	Update DMA Request Enable 0: Disable 1: Enable
15:9	Reserved		

17.6.3 State register (TMR6_STS)

Offset address: 0x10

Reset value: 0x0000

Field	Name	R/W	Description
0	UIFLG	RC_W0	Update Event Interrupt Generate Flag 0: Update event interrupt does not occur 1: Update event interrupt occurs When the counter value is reloaded or reinitialized, an update event will be generated. The bit is set to 1 by hardware and cleared by software; update events are generated in the following situations: (1) UD=0 on TMR6_CTRL1 register, and when the value of the repeat counter overruns/underruns, an update event will be generated; (2) URSSEL=0 and UD=0 on TMR6_CTRL1 register, configure UEG=1 on TMR6_CEG register to generate update event, and the counter needs to be initialized by software;
15:1	Reserved		

17.6.4 Control event generation register (TMR6_CEG)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
0	UEG	W	Update Event Generate 0: Invalid 1: Initialize the counter and generate the update event This bit is set to 1 by software, and cleared by hardware. Note: When an update event is generated, the counter of the prescaler will be cleared, but the prescaler factor remains unchanged.

Field	Name	R/W	Description
15:1	Reserved		

17.6.5 Counter register (TMR6_CNT)

Offset address: 0x24

Reset value: 0x0000

Field	Name	R/W	Description
15:0	CNT	R/W	Counter Value

17.6.6 Prescaler register (TMR6_PSC)

Offset address: 0x28

Reset value: 0x0000

Field	Name	R/W	Description
15:0	PSC	R/W	Prescaler Value Clock frequency of counter (CK_CNT)＝f_{CK_PSC}/(PSC+1).

17.6.7 Auto reload register (TMR6_AUTORLD)

Offset address: 0x2C

Reset value: 0xFFFF

Field	Name	R/W	Description
15:0	AUTORLD	R/W	Auto Reload Value When the value of auto reload is empty, the counter will not count.

18 Infrared Timer (IRTMR)

18.1 Introduction

IRTMR is an infrared interface for remote control, which can use an infrared LED to realize remote control function.

18.2 Functional Description

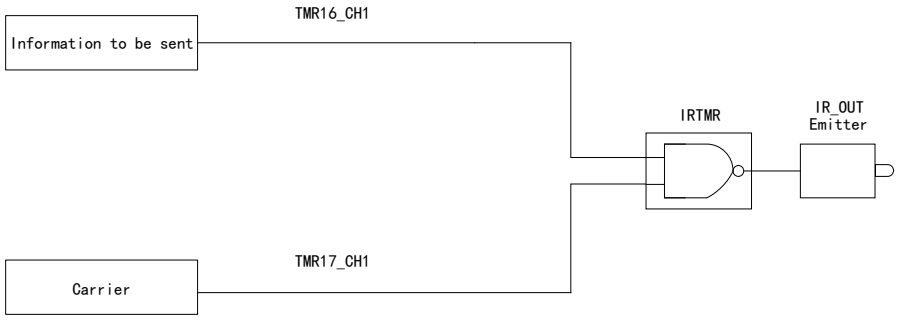
18.2.1 IRTMR Receive

The infrared receiver can be connected to the GPIO of the controller or the input capture channel of the timer through the output of the external IR receiver module to realize data receiving.

18.2.2 IRTMR Transmit

IRTMR is internally connected to TMR16 and TMR17, and the specific block diagram is as follows:

Figure 78 IRTMR Structure Block Diagram



In order to generate correct infrared remote control signal, TMR17_CH1 should be configured correctly to provide a high-frequency carrier signal, while TMR16 only needs to provide the information we send.

The final modulation signal is output through IR_OUT pin, and this function is activated by enabling the related multiplexing functions in GPIOx_ALFx register.

19 Watchdog Timer (WDT)

19.1 Introduction

The watchdog is used to monitor system failures caused by software errors. There are two watchdog devices on the chip: independent watchdog and window watchdog, which improve the security, and make the time more accurate and the use more flexible.

The independent watchdog will reset when the counter decreases to 0, and At the same time, before it goes down to zero, when the value on the counter is greater than the window value, it will be reset if it is reloaded.

The window watchdog will reset when the counter decreases to 0x3F. When the count value of the counter is before the window value of the configuration register, the refresh counter will also be reset.

19.2 Independent Watchdog Timer(IWDT)

19.2.1 Introduction

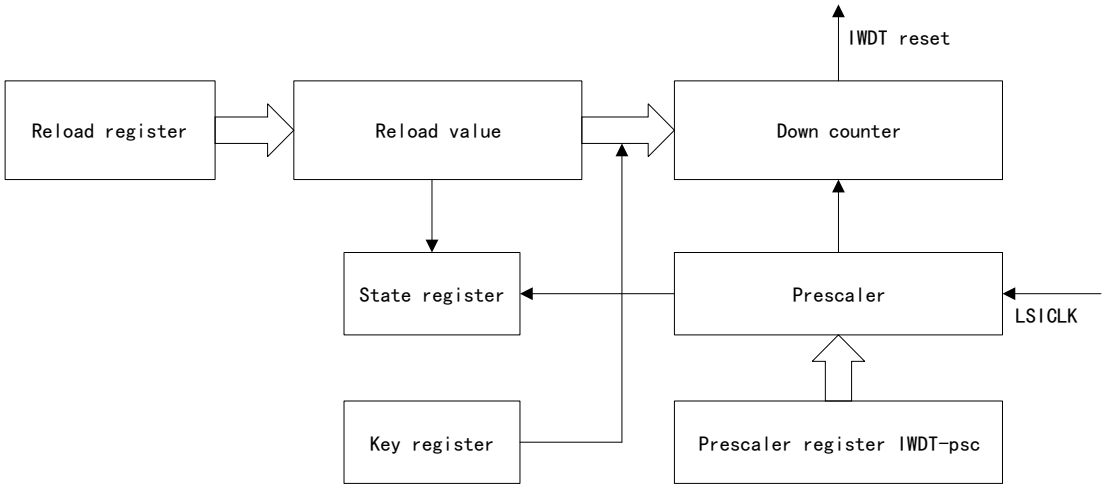
The independent watchdog consists of an 8-bit prescaler IWDT_PSC, 12-bit count-down counter, 12-bit reload register IWDT_CNTRLD, key register IWDT_KEY, state register IWDT_STS.

The independent watchdog has an independent clock source, and even if the master clock fails, it is still valid.

The independent watchdog is applicable to the situations where an independent environment is required but the accuracy requirement is not high.

19.2.2 Structure Block Diagram

Figure 79 Independent Watchdog Structure Block Diagram



Note: The prescaler, reload value and count-down counter are in V_{DD} power supply area; the prescaler register, status register, reload register and keyword register are in 1.2V power supply area. The watchdog function is in the V_{DD} power supply area and it can work normally in the stop or standby mode.

19.2.3 Functional Description

19.2.3.1 Key register

Write 0xCCCC in the key register to enable the independent watchdog, then the counter starts to count down from the reset value 0xFFF and when the counter counts to 0x000, a reset will be generated.

Write 0xAAAA in the key register, and the value of the reload register will be reloaded to the counter to prevent the watchdog from resetting.

Write 0X5555 in the key register to rewrite the value of the prescaler register, reload register and window value register.

19.2.3.2 Window register

The default value of Window register IWDT_WIN is 0xFFF. In the case of no update, the window option is disabled. When the window value is changed, the reload operation will be performed, and the watchdog counter value will be set to the value of IWDT_CNTRLD, which can delay the event cycle needed for reset.

The independent watchdog can work in the window watchdog mode, and the value of window register IWDT_WIN needs to be set appropriately.

19.2.3.3 Configuration IWDT

Configuration IWDT when window register is used

- Enable IWDT (write 0xCCCC to the key register IWDT_KEY)
- Open the register access permission (write 0x5555 to the key register IWDT_KEY)
- Configure IWDT_PSC prescaler register (write the value within 0~7 to IWDT_PSC)
- The value of wait state register IWDT_STS is updated to 0x00
- Configuration window register IWDT_WIN (the value of auto reload register IWDT_CNTRLD can be updated to the watchdog register)

Note: When the value of state regiser IWDT_STS is 0x00, the window value will be written to refresh the counter with the value of auto reload

Configuration IWDT when window register is disabled

- Enable IWDT (write 0xCCCC to the key register IWDT_KEY)
- Open the register access permission (write 0x5555 to the key register IWDT_KEY)
- Configure IWDT_PSC prescaler register (write the value within 0~7 to IWDT_PSC)
- Configuration reload register IWDT_CNTRLD
- The value of wait state register IWDT_STS is updated to 0x00
- Use IWDT_CNTRLD register to referesh the watchdog counter

19.2.3.4 Regiser access protection

The prescaler register IWDT_PSC, reload register IWDT_CNTRLD and window register IWDT_WIN have the function of write protection. If you want to rewrite these three registers, you need to write 0X5555 in the key register. If you write other value in the key register, the protection of the register will be started again.

Write 0xAAAA to the key register and the write protection function will also be enabled.

The prescaler register, reload register and window register can be observed through the state register.

19.2.3.5 Hardware watchdog

After the "hardware watchdog" function is enabled, and the system is powered on and reset, the watchdog will run automatically. If 0xAAAA is not written to the key register, reset will be generated after the counter finishes counting.

19.2.3.6 Debug mode

The independent watchdog can be configured in debug mode and choose to stop or continue to work. It depends on the IWDT_STS bit of DBGMCU_APB1F register in DBGMCU module.

19.3 Window Watchdog

19.3.1 Introduction

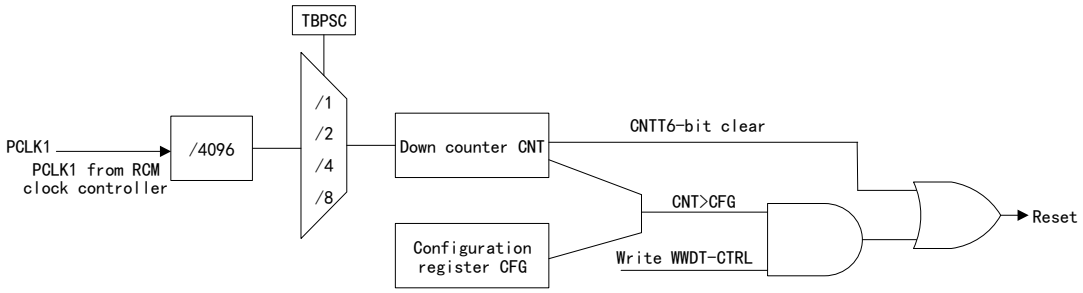
The window watchdog contains a 7-bit free-running down counter, prescaler and control register WWDT_CTRL, configuration register WWDT_CFG and state register WWDT_STS.

The window watchdog clock comes from PCLK, and the counter clock is obtained from the CK counter clock through frequency division by prescaler (configured by the configuration register).

The window watchdog is applicable when precise timing is needed.

19.3.2 Structure Block Diagram

Figure 80 Window Watchdog Structure Block Diagram



19.3.3 Functional Description

Enable window watchdog timer; the reset conditions are:

- When the counter count is less than 0x40, a reset will be generated.
- The reload counter will be reset before the counter counts to the value of the window register.

After reset, the watchdog is always closed and the watchdog can be enabled only by setting the WWDTEN bit of WWDT_CTRL control register.

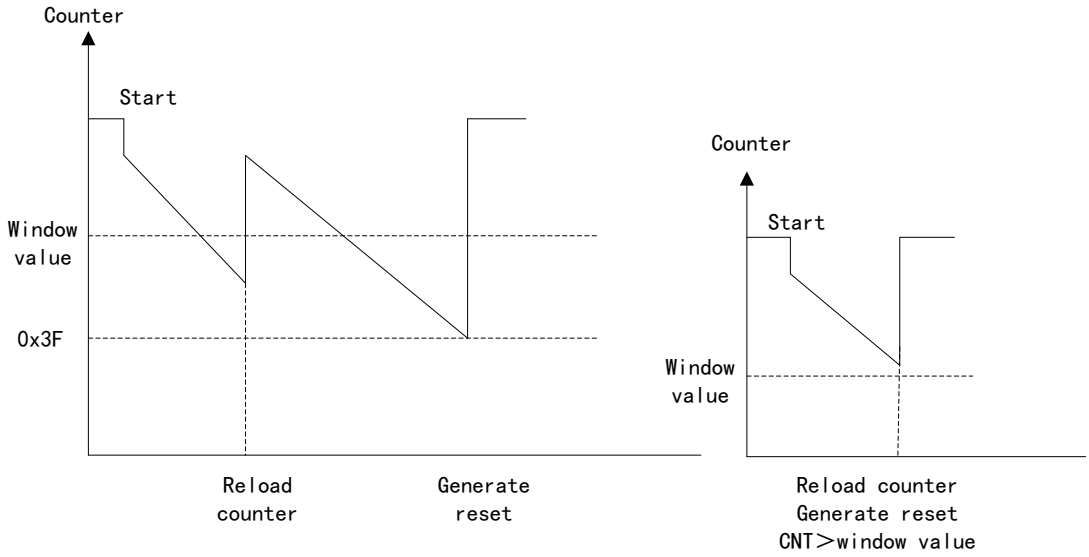
The counter of window watchdog is in free state. When the watchdog is disabled, the counter will continue to count down. The counter must be reloaded between the value of window register and 0x40 to avoid reset.

Setting the EWIEN bit of the configuration register can enable the early wake-up interrupt. When the count reaches 0x40, the interrupt will be generated. Entering the interrupt service program (ISTS) can be used to prevent the window watchdog from resetting. EWIEN interrupt can be cleared by writing 0 in the state register.

The unique window of the window watchdog timer can effectively monitor whether the program is faulty. For example, assuming that the running time of a program segment is T, and the value of the window register is slightly less than (TR-T), if

there is no reload register in the window, it means that the program is faulty, and when the counter counts to 0x3F, it will generate reset.

Figure 81 Window Watchdog Timing Diagram



The calculation formula of window watchdog timer timeout is as follows:

$$T_{WWDT}=T_{PCLK1}\times 4096\times 2^{TBPSC}\times (CNT[5:0]+1)$$

Wherein:

- T_{WWDT}: WWDT timeout
- T_{PCLK1}: Clock cycle of APB in ms
- If WIN[6:0] is less than or equal to 0x3F, the value is 0x3F

Table 55 Minimum/Maximum timeout when PCLK1=36MHz

TBPSC	Minimum timeout value	Maximum timeout value
0	113μs	7.28ms
1	227μs	14.56ms
2	455μs	29.12ms
3	910μs	58.25ms

19.3.3.1 Debug Mode

The window watchdog can be configured in debug mode and choose to stop or continue to work. It depends on the WWDT_STS bit of DBGMCU_APB1F register in DBGMCU module.

19.4 IWDT Register Address Mapping

Table 56 IWDT Register Mapping

Register name	Description	Offset address
IWDT_KEY	Key register	0x00

Register name	Description	Offset address
IWDT_PSC	Prescaler register	0x04
IWDT_CNTRLD	Counter reload register	0x08
IWDT_STS	State register	0x0C
IWDT_WIN	Window register	0x10

19.5 IWDT Register Functional Description

These peripheral registers can be operated by half word (16 bits) or word (32 bits).

19.5.1 Key register (IWDT_KEY)

Offset address: 0x00

Reset value: 0x0000 0000 (reset in standby mode)

Field	Name	R/W	Description
15:0	KEY	W	Allow Access IWDT Register Key Value Writing 0x5555 means enabled access to IWDT_PSC, IWDT_CNTRLD and IWDT_WIN registers.When the software writes 0xAAAA, it means to execute the reload counter, and a certain interval is required to prevent the watchdog from resetting. Write 0xCCCC and the watchdog will be enabled (the hardware watchdog is unrestricted by this command word). The register only writes, read-out value is 0x0000.
31:16	Reserved		

19.5.2 Prescaler register (IWDT_PSC)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	PSC	R/W	Prescaler Factor Configure Support write protection function; when writing 0x5555 in the IWDT_KEY register, it is allowed to access the register; in the process of writing this register, only when IWDT_STS register PSCUFLG=0, can the prescaler factor be changed; in the process of reading this register, only when PSCUFLG=0, can the read-out value of PSC register be valid. 000：PSC=4 001：PSC=8 010：PSC=16 011：PSC=32 100：PSC=64 101：PSC=128 110：PSC=256 111：PSC=256
31:3	Reserved		

19.5.3 Counter reload register (IWDT_CNTRLD)

Offset address: 0x08

Reset value: 0x0000 0FFF(reset in standby mode)

Field	Name	R/W	Description
11:0	CNTRLD	R/W	Watchdog Counter Reload Value Setup It supports write protection function and defines the value loaded to the watchdog counter when 0xAAAA is written by IWDT_KEY register; in the process of writing this register, this register can be modified only when CNTUFLG=0. In the process of reading this register, when CNTUFLG=0 in IWDT_STS register, the read value is valid. The watchdog timeout cyclecan be calculated by the reload value and clock prescaled value.
31:12	Reserved		

19.5.4 State register (IWDT_STS)

Offset address: 0x0C

Reset value: 0x0000 0000 (not reset in standby mode)

Field	Name	R/W	Description
0	PSCUFLG	R	Watchdog Prescaler Value Update Flag When the prescaler factor is updated, it is set to 1 by hardware; after the prescaler factor is updated, the bit is cleared by hardware; the prescaler factor is updated only when the PSCUFLG bit is cleared.
1	CNTUFLG	R	Watchdog Counter Reload Value Update Flag When the counter reload value is updated, it is set to 1 by hardware; after the counter reload value is updated, the bit is cleared by hardware; the counter reload value is updated only when the CNTUFLG bit is cleared.
2	WINUFLG	R	Watchdog Counter Window Value Update Flag When the window value is updated, it is set to 1 by hardware; after the window value of the counter is updated, the bit is cleared by hardware; the window value is valid only when the IWDT_WIN register is enabled.
31:3	Reserved		

19.5.5 Window register (IWDT_WIN)

Offset address: 0x10

Reset value: 0x0000 0FFF(reset in standby mode)

Field	Name	R/W	Description
11:0	WIN	R/W	Watchdog Counter Window Value These bits include the window value and the initial value of down counter These bits can be modified only when STS_WINUFLG=0,Reloading the counter between the counter value and the window value can prevent resetting Note: When reading this register, the value of V_{DD} power supply domain will be returned, so if you want to read data, you should ensure STS_WINUFLG=0.
31:12	Reserved		

Note: When the reload setting, prescaler setting and window value resetting are running, if you want to change the reload value, prescaler value and window value, you need to confirm that the relevant flag bits are 0. There is no need to wait after the update, unless you want to enter the low-power mode.

19.6 WWDT Register Address Mapping

Table 57 WWDT Register Address Mapping

Register name	Description	Offset address
WWDT_CTRL	Control register	0x00
WWDT_CFG	Configuration register	0x04
WWDT_STS	State register	0x08

19.7 WWDT Register Functional Description

These peripheral registers can be operated by half word (16 bits) or word (32 bits).

19.7.1 Control register (WWDT_CTRL)

Offset address: 0x00

Reset value: 0x0000 007F

Field	Name	R/W	Description
6:0	CNT	R/W	Counter Value Setup This counter is 7 bits, and CNT6 is the most significant bit These bits are used to store the counter value of the watchdog. When the count value decreases from 0x40 to 0x3F, WWDT reset will be generated.
7	WWDTEN	R/S	Window Watchdog Enable This bit is set to 1 by software and can be cleared by hardware only after reset. When WWDTEN=1, WWDT can generate a reset. 0: Disable 1: Enable
31:8	Reserved		

19.7.2 Configuration register (WWDT_CFG)

Offset address: 0x04

Reset value: 0x0000 007F

Field	Name	R/W	Description
6:0	WIN	R/W	Window Value Setup This window value is 7 bits, which is used to compare with the down counter.
8:7	TBPSC	R/W	Configure the time base prescaler factor (Timer Base Prescaler Factor Configure) Divide the frequency on the basis of PCLK1/4096 00: No frequency division 01: 2-divided frequency 10: 4-divided frequency 11: 8-divided frequency
9	EWIEN	R/S	Early Wakeup Interrupt Enable 0: Meaningless 1: When the counter value reaches 0x40, an interrupt will be generated; this interrupt is cleared by hardware after reset.

Field	Name	R/W	Description
31:10	Reserved		

19.7.3 State register (WWDT_STS)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	EWIFLG	RC_W0	Early Wakeup Interrupt Occur Flag 0: Not occur 1: When the counter value reaches 0x40, it is set to 1 by hardware; if the interrupt is not enabled, the bit will also be set to 1. It can be cleared by writing 0 by software Writing 1 to this bit is invalid.
31:1	Reserved		

20 Real-time clock (RTC)

20.1 Full Name and Abbreviation Description of Terms

Table 58 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Second	SEC
Alarm	ALR
Prescaler	PSC

20.2 Introduction

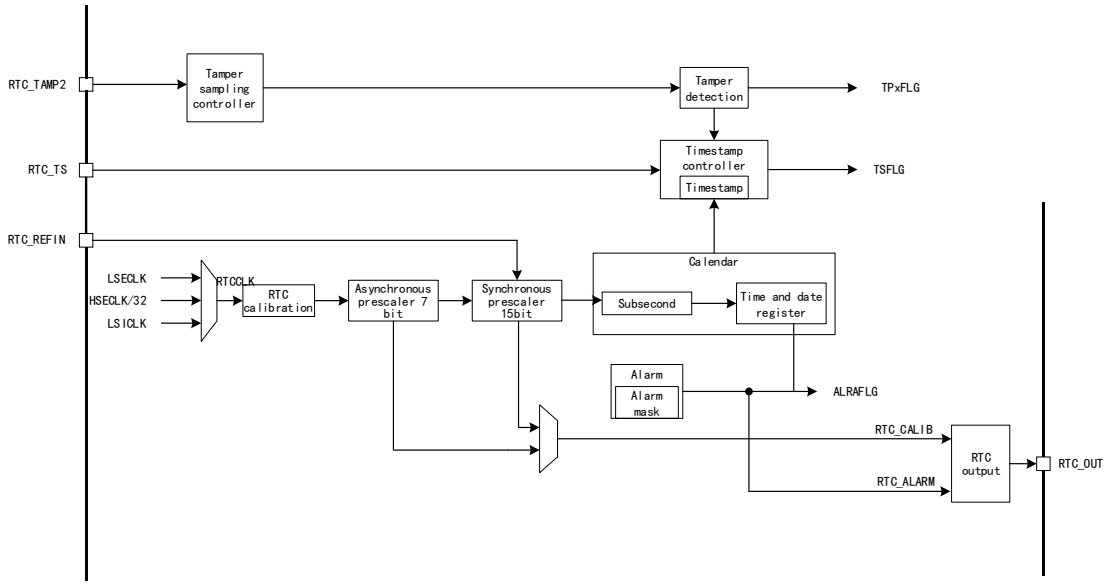
It has sub-second, time and date registers with BCD coding, as well as corresponding alarm registers, and can realize timestamp function together with external pins. It supports clock calibration function and time compensation.

20.3 Main Characteristics

- Timebase unit
- Clock calibration
- Subsecond, time and date
- Time error compensation
- Alarm (subsecond, time and date mask)
- Timestamp
- Tamper detection
- 3 kinds of RTC outputs
- Multiple interrupt control
- Automatic wakeup of low power

20.4 Structure Block Diagram

Figure 82 RTC Structure Block Diagram



Note:

1) Alternate function output: RTC_OUT is output in one of the following two forms
   - RTC_CALIB: This output is enabled through CALOEN bit of RTC_CTRL register, and when the frequency of LSECLK is 32.768kHz, the clock output is 512Hz or 1Hz.
   - RTC_ALARM: This output, Alarm A, is enabled through OUTSEL bit of RTC_CTRL register.
2) Alternate function input:
   - RTC_TS: Timestamp event
   - RTC_TAMP2: Tamper event detection 2
   - RTC_REFIN: 50 or 60 reference clock inputs

20.5 Functional Description

20.5.1 I/O Pin Controlled by RTC

RTC_OUT, and RTC_TS in RTC can be mapped to the same pin (PC13).

The output selection of RTC_ALARM is configured through RTC_TACFG, and PC13VAL bit of RTC_TACFG register is used to select RTC_ALARM to configure push-pull output or open-drain output.

When PC13 pin does not use RTC alternate function, PC13 pin is forced to be push-pull output by setting PC13EN bit of RTC_TACFG register; PC13VAL bit is used to set the value of PC13 pin output data. Then the push-pull output and data value of PC13 pin can be maintained in standby mode.

The following table shows the priority sequence followed by the output mechanism:

Table 59 PC13 Pin Controlled by RTC

Pin configuration and function	RTC_ALARM Output enable	RTC_CALIB Output enable	RTC_TS Input enable	PC13EN	PC13VAL
RTC_ALARM Open-drain output	1	No effect	No effect	No effect	0
RTC_ALARM Push-pull output	1	No effect	No effect	No effect	1
RTC_CALIB Push-pull output	0	1	No effect	No effect	No effect
RTC_TS Floating input	0	0	1	No effect	No effect
RTC_TS Floating input	0	0	1	No effect	No effect
Forced to push-pull output	0	0	0	1	PC13 output data value
Wake-up pin or standard GPIO	0	0	0	0	No effect

When PC14 and PC15 do not use LSECLK oscillator, PC14/PC15 can be forced to be push-pull output by setting PC14EN and PC15EN bits of RTC_TACFG register; PC14VAL and PC15VAL bits set the output data, and the push-pull output and data value of PC14 and PC15 can be maintained in standby mode.

The following table shows the priority sequence followed by the output mechanism:

Table 60 PC14 Pin Controlled by LSECLK

Pin configuration and function	RCM_RTCCTRL LSEEN bit of register	RCM_RTCCTRL LSEBCFG bit of register	PC14EN	PC14VAL
LSECLK oscilltor	1	0	No effect	No effect
LSECLK bypass	1	1	No effect	No effect
Forced to push-pull output	0	No effect	1	PC14 output data value
Standard GPIO	0	No effect	0	No effect

Table 61 PC15 Pin Controlled by LSECLK

Pin configuration and function	RCM_RTCCTRL LSEEN bit of register	RCM_RTCCTRL LSEBCFG bit of register	PC15EN	PC15VAL
LSECLK oscilltor	1	0	No effect	No effect
Forced to push-pull output	1	1	1	PC15 output data value
	0	No effect	1	
Standard GPIO	0	No effect	0	No effect

20.5.2 Timebase Unit

Clock source

RTC has three clock sources RTC_CLK:

- External LSECLK crystal oscillator
- Internal LSICLK
- 32 frequency division of external HSECLK crystal oscillator

Different clock sources are configured using the RTCSRCSEL of the RCM_RTCCTRL register of the clock controller RCM.

Prescaler

The power consumption of RTC peripheral should be minimized as far as possible. In order to give consideration to the power consumption, dual prescalers, 7bit asynchronous prescaler APSC and 15bit synchronous prescaler SPSC are used in RTC.

RTC_CLK first passes through the asynchronous prescaler, and the clock after frequency division reaches the synchronous prescaler. Two prescalers can be reasonably configured to generate a 1Hz clock for calendar.When the prescaler is used, it is suggested that the asynchronous prescaler should be adjusted as high as possible to reduce power consumption.The synchronous prescaled value can also be used as the reload value of the subsecond counter.

20.5.3 Clock Calibration

Clock synchronization

RTC can realize clock synchronization according to external high-precision clcok and the register RTC_SHIFT. The deviation between RTC clock and external clock is detected mainly by acquiring the timestamps of subsecond time period twice. Since the synchronous prescaled value is used as the reload value of the subsecond counter, and the SFSEC bit of register RTC_SHIFT is used in the subsecond counter, the SFSEC bit can be adjusted to finely tune the RTC clock and increase or decrease several cycles artificially.

Reference clock

RTC has internal reference clock detection, which can be used to compensate the deviation of external LSECLK crystal oscillator. Set RCLKDEN bit to enable the reference clock detection, compare the external 50Hz or 60Hz reference clock with the internal 1Hz clock of RTC through RTC_REFIN pin, and through this mechanism, the 1Hz clock after LSECLK frequency division is automatically compensated.

After the reference clock detection is enabled, the synchronous and asynchronous prescaler of the clock unit must be configured as the default value.The reference clock detection cannot be used simultaneously with the clock synchronization, and it should be disabled in standby mode.

RTC digital calibration

RTC uses 2^{20} RTC_CLK as a calibration cycle by default. In addition, 2^{19} and 2^{18} RTC_CLK can be set as a calibration cycle through the registers CALW16 and CALW8. When LSECLK is used as RTC_CLK clock source, the calibration cycle of RTC is 32s, 16s, 8s.

- 16s calibration cycle; the hardware sets RECALF[0] to '0'
- 8s calibration cycle; the hardware sets RECALF[1:0] to '00'

Take 32s calibration cycle as an example, the calibration mechanism is to add or reduce some RTC_CLK signals in the calibration cycle.

- When RECALF is used, RECALF RTC_CLK are reduced every 2^{20} RTC_CLK
- When ICALFEN is used and ICALFEN=1, one RTC_CLK is added every 2^{11} RTC_CLK
- When RECALF is used and ICALFEN, (512 * ICALFEN - RECALF) RTC_CLK are added every 2^{20} RTC_CLK

20.5.4 RTC Write Protection

In order to prevent counting exception caused by accidental write, RTC register adopts write protection mechanism. Only when the write protection is removed, can the register with write protection function be operated.

After power-on, RTC register will enter the write protection state and the protection cannot be removed by system reset. The write protection can be removed by writing special keywords '0xCA' and '0x53' to the register RTC_WRPROT. If the wrong keyword is written, RTC will immediately enable write protection.

20.5.5 Calendar Register

RTC has subsecond, time and date shadow registers encoded by BCD, which are RTC_SUBSEC, RTC_TIME and RTC_DATE respectively. The current calendar can be obtained by accessing the shadow register or obtained directly from the calendar counter. The time system of 24 hours and 12 hours can be selected by TIMEFCFG bit of configuration register RTC_CTRL.

RTC updates the shadow register every two RTC_CLK cycles, and sets the flag bit RSFLG. When waking up from shutdown or standby mode, generally the shadow register will not be updated, which requires waiting for up to two RTC_CLK cycles. The reset of shadow register is caused by system reset.

The shadow register is synchronized with f_{APB1}.

The way to read the calendar can be selected by RCMCFG bit of configuration register RTC_CTRL.

RCMCFG=0, read the calendar from the shadow register

In this mode, it is recommended that f_{APB1} is greater than 7*fRTC_CLK.

After the shadow register is updated, the flag bit RSFLG will be set. The software can read the calendar only after the bit RSFLG is set. Every time the calendar is read, the RSFLG flag should be cleared manually. To ensure the normal reading of calendar value, it is required to read the shadow register twice. If the calendar obtained twice is the same, the calendar is read successfully.

When waking up from stop or standby mode, since the shadow register is not updated, the RSFLG flag should be cleared immediately.

RCMCFG=1, read the calendar from the calendar counter

When f_{APB1} is less than 7*fRTC_CLK or the system is woken from low-power mode, it is recommended to read the calendar directly from the calendar counter.

If RSFLG bit is not set to 1 when reading the calender just at the stage of calendar

counter change, it is required to read the calendar twice. Therefore, it is also recommended to read the calendar counter twice. When the read calendar value is the same twice, it means that the calendar is read successfully.

20.5.6 Time Compensation

Due to seasonal changes, time compensation is sometimes needed to make it more suitable for daily needs. RTC is integrated with time compensation unit and its summer time flag. Users can choose whether to turn on time compensation according to their own needs.

By setting STCCFG bit of the register RTC_CTRL, the summer time will increase by 1 hour; by setting WTCCFG bit of the register RTC_CTRL, the winter time will will decrease by 1. BAKP flag is used to record whether the summer time is set.

20.5.7 Programmable Alarm

As a real-time clock, RTC integrates alarm function, and it runs mainly through alarm cock configuration register and alarm mask, in combination with calendar counter.

Configure the alarm and alarm mask through the register RTC_ALRMA、RTC_ALRMASS, and the alarm mask informs RTC to pay attention to the time period of the alarm. After the alarm function is enabled, the alarm will be triggered only when the concerned time period reaches the set value. At this time, the alarm flag is set. If the alarm interrupt is enabled, the interrupt processing will be triggered.

Select "seconds" as the time period of the alarm, and only when the synchronous prescaler value is greater than 2, can the alarm operate normally.

20.5.8 Timestamp

RTC supports timestamp function and the RTC_TS pin works together with the timestamp register.

The timestamp polarity is detected through TSETECFG bit of the register RTC_CTRL. When RTC_TS pin recognizes the external timestamp edge signal, RTC will automatically latch the current calendar in the subsecond, time and date timestamp registers, and the timestamp flag bit TSFLG will be set to 1. If the timestamp interrupt is enabled, the timestamp interrupt processing will be triggered.

When TSFLG flag bit is set to 1, and a timestamp event occurs, the timestamp will overrun, and the flag bit TSOVRFLG will be set to 1. If a timestamp event is detected once TSFLG flag is cleared, both TSFLG and TSOVRFLG flags will be set to 1.

20.5.9 Tamper Detection

Tamper detection is a kind of data self-destruction protection device to prevent data leakage caused by tamper. Through the hardware circuit design, the tamper detection signal is transmitted to the tamper detection pin.

Tamper detection has multiple tamper detection pins, and each pin is enabled by a register bit separately. In order to detect real tamper events better, signal filtering can be configured, and tamper detection polarity can be configured for each pin.

Tamper detection polarity

The low level/rising edge and high level/falling edge can be selected as tamper detection polarity through TPxALCFG bit in the register RTC_TACFG.

Tamper signal filter

TPSFSEL bit of the register RTC_TACFG is used to configure the sampling frequency of tamper detection, and TPFCSEL bit of RTC_TACFG is used to configure after how many valid tamper signals are detected continuously, a tamper event can be generated.

In particular, if a tamper signal has been generated on the tamper detection pin before the tamper detection pin is enabled, a tamper event will be immediately generated on the enabled tamper detection pin.

Tamper timestamp

At some times, in order to record the tamper detection events, RTC can latch the current tamper timestamp and this function can be enabled quickly through TPTSEN bit of the register RTC_TACFG, not needing to enable the timestamp function additionally.

20.5.10 Automatic Wake-up

Compared with RTC alarm, the hardware structure of the automatic wake-up is simpler, and it has no complicated configuration process of RTC alarm, so it is a good scheme to wake up the low power consumption.

There is a 16bit self-decrement reload counter in RTC, and it is used to wake up the device automatically.

The clock of this counter is selected by WUCLKSEL bit of the register RTC_CTRL, and by selecting different clocks, the automatic wake-up cycle can be configured from 122μs to 36h. First turn off the automatic wake-up, namely, clear WUTEN; when WUTWFLG flag bit is set to 1, configure WUCLKSEL bit of the RTC_CTRL register and the reload register RTC_AUTORLD.

When the counter decreases to 0, a wake-up event will be generated, WUTFLG flag bit will be set to 1, and before entering the next round of automatic wake-up, this flag bit must be cleared.

20.5.11 RTC Output

RTC output transmits the internal RTC calibration clock, alarm signal, and automatic wake-up signal to the outside through PC13 pin.

RTC calibration clock

Calibration clock output is generally used to observe the accuracy of RTC clock source, and the observed value is used to calibrate the clock source. 512Hz and 1Hz signal output sources can be selected through CALOSEL bit of RTC_CTRL register, and CALOEN bit of RTC_CTRL register can enable the calibration output.

Alarm and automatic wake-up signal

When the alarm or automatic wake-up is running, these two events can be output as pulse signals. OUTSEL bit of RTC_CTRL register is used to select the signal output source, and POLCFG bit is used to configure the output polarity.

20.6 Register Address Mapping

Table 62 RTC Register Address Mapping

Register name	Description	Offset address
RTC_TIME	RTC time register	0x00
RTC_DATE	RTC date register	0x04
RTC_CTRL	RTC control register	0x08
RTC_STS	RTC state register	0x0C
RTC_PSC	RTC prescaler register	0x10
RTC_AUTORLD	RTC auto reload register	0x14
RTC_ALRMA	RTC alarm A register	0x1C
RTC_WRPROT	RTC write protection register	0x24
RTC_SUBSEC	RTC subsecond register	0x28
RTC_SHIFT	RTC shift register	0x2C
RTC_TSTIME	RTC timestamp time register	0x30
RTC_TSDATE	RTC timestamp date register	0x34
RTC_TSSUBSEC	RTC timestamp subsecond register	0x38
RTC_CAL	RTC calibration register	0x3C
RTC_TACFG	RTC tamper and multiplexing configuration register	0x40
RTC_ALRMASS	RTC alarm A subsecond register	0x44

20.7 Register Functional Description

20.7.1 RTC time register (RTC_TIME)

RTC_TIME is calendar time shadow register, and this register can be written only in initialization mode and is in write protection state.

Offset address: 0x00

Power-on reset value: 0x0000 0000

System reset value: 0xXXXX XXXX

Field	Name	R/W	Description
3:0	SECU	R/W	Second Ones Unit in BCD Format Setup
6:4	SECT	R/W	Second Ten's Place Unit in BCD Format Setup
7	Reserved		
11:8	MINU	R/W	Minute Ones Unit in BCD Format Setup
14:12	MINT	R/W	Minute Ten's Place Unit in BCD Format Setup
15	Reserved		
19:16	HRU	R/W	Hour Ones Unit in BCD Format Setup

Field	Name	R/W	Description
21:20	HRT	R/W	Hour Ten's Place Unit in BCD Format Setup
22	TIMEFCFG	R/W	Time Format 0: AM or 24-hour system 1: PM
31:23	Reserved		

20.7.2 RTC date regiter (RTC_DATE)

RTC_DATE is calendar date shadow register, and this register can be written only in initialization mode and is in write protection state.

Offset address: 0x04

Reset value: 0x0000 2101

Field	Name	R/W	Description
3:0	DAYU	R/W	Day Ones Unit in BCD Format Setup
5:4	DAYT	R/W	Day Ten's Place Unit in BCD Format Setup
7:6	Reserved		
11:8	MONU	R/W	Month Ones Unit in BCD Format Setup
12	MONT	R/W	Month Ten's Place Unit in BCD Format Setup
15:13	WEEKSEL	R/W	Week Day Units Select 000: Disable 001: Monday ... 111: Sunday
19:16	YRU	R/W	Year Ones Unit in BCD Format Setup
23:20	YRT	R/W	ear Ten's Place Unit in BCD Format Setup
31:24	Reserved		

20.7.3 RTC control register (RTC_CTRL)

（1） The bits 7, 6 and 4 of this register can be written only in initialization mode.

（2） It is not recommended to rewrite this register when the number of hours in the calendar increases, which is because the correct increment of hours may be masked.

（3） The written values of STCCFG and WTCCFG will take effect from next second.

（4） This register is under write protection.

Offset address: 0x08

Power-on reset value: 0x0000 0000

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
2:0	WUCLKSEL	R/W	Wakeup Clock Select 000：RTC/16 001：RTC/8 010：RTC/4 011：RTC/2 10x：clk_spre (usually 1Hz)

Field	Name	R/W	Description
			11x：clk_spre (usually 1Hz) and add 2^{16} to WUAUTORE counter value
3	TSETECFG	R/W	Time Stamp Event Trigger Edge Configure This bit indicates that RTC_TS generates a timestamp event on rising edge or falling edge. 0: Rising edge 1: Falling edge This bit will be changed when TSEN=0.
4	RCLKDEN	R/W	RTC_REFIN reference clock detection enable 0: Disable 1: Enable SPSC must be 0x00FF
5	RCMCFG	R/W	Read Calendar Value Mode Configure 0: The calendar value is read from the shadow register, and the shadow register is updated every two RTCCLK cycles 1: The calendar value is read from the calendar counter If the clock frequency of APB1 is lower than seven times of RTCCLK frequency, RCMCFG must be set to 1.
6	TIMEFCFG	R/W	Time Format Configure 0: 24-hour/day format 1: AM/PM time format
7	Reserved		
8	ALREN	R/W	Alarm A Function Enable 0: Disable 1: Enable
9	Reserved		
10	WUTEN	R/W	Wakeup Timer Enable 0: Disable 1: Enable
11	TSEN	R/W	Time Stamp Enable 0: Disable 1: Enable
12	ALRIEN	R/W	Alarm A Interrupt Enable 0: Disable 1: Enable
13	Reserved		
14	WUTIEN	R/W	Wakeup Timer Interrupt Enable 0: Disable 1: Enable
15	TSIEN	R/W	Time Stamp Interrupt Enable 0: Disable 1: Enable
16	STCCFG	R/W	Summer Time Change Configure The bit will always be 0 in the reading process; if this bit is set not in the initialization mode, the calendar time will increase by 1. 0: Invalid 1: The current time increases by 1 hour to calibrate the summer time variation
17	WTCCFG	R/W	Winter Time Change Configure The bit will always be 0 in the reading process; if this bit is set not in the initialization mode, and HRx of RCT_TIME register is 0, this bit is invalid, and if HRx is not 0, the calendar time will decrease by 1. 0: Invalid 1: The current time increases by 1 hour to calibrate the winter time variation
18	BAKP	R/W	Backup Value Setup This bit indicates whether the summer time has changed and is written by the user.
19	CALOSEL	R/W	Calibration Output Value Select When CALOEN=1, this bit is used to select the output signal of RTC_CALIB. 0: 512Hz 1: 1Hz

Field	Name	R/W	Description
			The above frequency is valid when RTCCLK is 32.768kHz and the prescaler is at the default value (APSC=127, SPSC=255).
20	POLCFG	R/W	Output Polarity Configure This bit indicates the level state of the pin when ALRAF/WUTFLG bit is set to 1 (depending on OUTSEL bit). 0: High level 1: Low level
22:21	OUTSEL	R/W	Output Way Select This bit is used to select the flag bit associated with RTC_ALARM output 00: Output is disabed 01: Alarm A output is enabled 10: Reserved 11: Wake-up output is enabled
23	CALOEN	R/W	Calibration Output Enable This bit is used to enable RTC_CAL output 0: Disable 1: Enable
31:24	Reserved		

20.7.4 RTC state register (RTC_STS)

This register (except RTC_STS[13:8] bit) is in write protection state.

Offset address: 0x0C

Power-on reset value: 0x0000 0007

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
0	ALRWFLG	R	Alarm A Write Occur Flag When ALREN=0 for RTC_CTRL, the value of alarm A will change and this bit will be set to 1 by hardware; this bit will be cleared by hardware in initialization mode. 0: The alarm A can be updated 1: The alarm A cannot be updated
1	Reserved		
2	WUTWFLG	R	Wakeup Timer Write Occur Flag When WUTEN=0, this bit is set to 1 by hardware after two RTCCLK cycles are set; after WUTEN=1, this bit is cleared after two RTCCLK cycles; When WUTEN=0 and WUTWFLG=1, the value of wake-up timer can be changed. 0: It is not allowed to update the wake-up timer configuration 1: It is allowed to update the wake-up timer configuration
3	SOPFLG	R	Shift Operation Pending Occur Flag 0: Not occur 1: Occurred When a shift operation is generated by writing to RTC_SHIFT register, this bit will be set to 1 by hardware immediately. After corresponding shift operation is performed, this bit will be cleared by software. It is invalid to write to SOPFLG.
4	INITSFLG	R	Initialization State Occur Flag When the "year" field in the calendar is not "0", this bit will be set by hardware. 0: Not occur 1: Occurred

Field	Name	R/W	Description
5	RSFLG	RC_W0	Registers Synchronization Occur Flag When the content in the calendar register is copied to the shadow registers (RTC_SUBSEC, RTC_TIME and RTC_DATE), this bit is set to 1 by hardware; when shifting operation is pending (SOPFLG=1) or is in the mode that the shadow register is ignored (RCMCFG=1), this bit is cleared by hardware in initialized mode; or this bit can be cleared by software. This bit is cleared by hardware/software in initialization mode. 0: Not synchronized 1: Synchronized
6	RINITFLG	R	Register Initialization Occur Flag This bit is set to "1", RTC is in initialization state, and the time, date and prescaler registers can be updated. 0: Cannot be initialized 1: Initialized
7	INITEN	R/W	Initialization Mode Enable 0: Free run mode 1: Initialization mode; it is used to program RTC_TIME, RTC_DATE and RTC_PSC. The counter stops counting, and after INITEN is reset, the counter will start counting from a new value.
8	ALRAFLG	RC_W0	Alarm A Match Occur Flag When RTC_TIME and RTC_DATE match the alarm A register RTC_ALRMA, this flag is set by hardware. This flag can be cleared by writing 0 by software.
9	Reserved		
10	WUTFLG	RC_W0	Wakeup Timer Occur Flag When the auto refresh counter counts to 0, this bit will be set to 1 by hardware; it is cleared by writing 0 by software. Clear this flag 1.5 RTCCLK cycles before WUTFLG is set to 1 again.
11	TSFLG	RC_W0	Time Stamp Occur Flag When a timestamp event occurs, this flag is set to 1 by hardware; it is cleared by writing 0 by software.
12	TSOVRFLG	RC_W0	Time Stamp Overflow Occur Flag When TSFLG=1 and a timestamp event is generated, this flag bit is set to 1 by hardware; it is cleared by writing 0 by software. It is recommended to clear this bit after TSFLG flag bit is cleared.
13	TP1FLG	RC_W0	RTC_TP1FLG Detection Occur Flag When a tamper event is detected in RTC_TP1FLG input, this flag is set to 1 by hardware, it can be cleared by writing 0 by software.
14	TP2FLG	RC_W0	RTC_TP2FLG Detection Occur Flag When a tamper event is detected in RTC_TP2FLG input, this flag is set to 1 by hardware, it can be cleared by writing 0 by software.
15	Reserved		
16	RCALPFLG	R	Recalibration Pending Occur Flag When the software writes to RTC_CAL, this bit is set to 1 automatically, and the RTC_CAL register is locked. This bit will return 0 when other new calibration setting is performed.
31:17	Reserved		

20.7.5 RTC prescaler register (RTC_PSC)

The register can only be written in the initialization mode, and the initialization must be completed by two independent write accesses, which is in write protected state.

Offset address: 0x10

Power-on reset value: 0x007F 00FF

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
14:0	SPSC	R/W	Synchronous Prescaler Coefficient ck_spre frequency=ck_apre frequency/(SPSC+1)
15	Reserved		
22:16	APSC	R/W	Asynchronous Prescaler Coefficient ck_apre frequency=RTCCLK frequency/(APSC+1)
31:23	Reserved		

20.7.6 RTC auto reload register (RTC_AUTORLD)

This register can be written only when WUTEFLG of RTC_STS is set to 1, and it is in write protection state.

Offset address: 0x14

Power-on reset value: 0x0000 FFFF

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
15:0	WUAUTORE	R/W	Wakeup Auto-reload Value Setup When the wake-up counter is waken up (WUTEN=1), this flag bit will be set to 1 in each CLK_WUAUTORE cycle, and CLK_WUAUTORE cycle can be set by WUCLKSEL bit of RTC_CTRL register. When WUCLKSEL[2]=1, the wake-up counter will be set to 17 bits, WUCLKSEL[1] is WUAUTORE[16], and is the most high bit reloaded to the timer. After setting WUTEN, the first set of WUTFLG "1" occurs when the first loop of CLK_WUAUTORE ends; WUAUTORE[15:0] is not configured to 0x0000 when WUCLKSEL[2:0]=011(RTCCLK/2) is slave.
31:16	Reserved		

20.7.7 RTC alarm A register (RTC_ALRMA)

This register can be written only when ALRWFLG of RTC_STS is set to 1 or in initialization mode, and it is in write protection state.

Offset address: 0x1C

Power-on reset value: 0x0000 0000

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
3:0	SECU	R/W	Second Ones Unit in BCD Format Setup
6:4	SECT	R/W	Second Ten's Place Unit in BCD Format Setup
7	SECMEN	R/W	Alarm A Seconds Mask Enable 0: If the "second" matches, set Alarm A 1: Mask the effect of the "second" value on Alarm A
11:8	MINU	R/W	Minute Ones Unit in BCD Format Setup
14:12	MINT	R/W	Minute Ten's Place Unit in BCD Format Setup
15	MINMEN	R/W	Alarm A Minutes Mask Enable 0: If the "minute" matches, set Alarm A 1: Mask the effect of the "minute" value on Alarm A
19:16	HRU	R/W	Hour Ones Unit in BCD Format Setup

Field	Name	R/W	Description
21:20	HRT	R/W	Hour Ten's Place Unit in BCD Format Setup
22	TIMEFCFG	R/W	Time Format Configure 0: AM or 24-hour system 1: PM
23	HRMEN	R/W	Alarm A Hours Mask Enable 0: If the "hour" matches, set Alarm A 1: Mask the effect of the "hour" value on Alarm A
27:24	DAYU	R/W	Day Ones Unit in BCD Format Setup
29:28	DAYT	R/W	Day Ten's Place Unit in BCD Format Setup
30	WEEKSEL	R/W	Week Day Select 0: DAYU means date 1: DAYU means the number of weeks. DAYT[1:0] has no effect.
31	DATEMEN	R/W	Alarm A Date Mask Enable 0: If the date/week matches, set Alarm A 1: Mask the effect of the date/week value on Alarm A

20.7.8 RTC write protection register (RTC_WRPROT)

Offset address: 0x24

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	KEY	W	Write Protection Key Value Setup This byte is written by softwre; read this byte and it is always 0x00. After writing 0xCA and 0x53, the RTC register write protection is removed. When other values are written, the RTC register enters a write protected state.
31:16	Reserved		

20.7.9 RTC subsecond register (RTC_SUBSEC)

Offset address: 0x28

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	SUBSEC	R	Sub Second Value Setup SUBSEC is the value of synchronous prescaler counter. It is determined by the following formula: Subsecond value=(SPSC-SUBSEC)/(SPSC+1) After one shift operation is performed, SUBSEC may be greater than SPSC. The correct time/date is one second less than RTC_TIME/RTC_DATE.
31:16	Reserved		

20.7.10 RTC shift register (RTC_SHIFT)

This register is in write protection state.

Offset address: 0x2C

Power-on reset value: 0x0000 0000

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
14:0	SFSEC	W	Subtract a Fraction of a Second Setup This bit field can only be written; read this byte and it is always 0. Writing to this bit is invalid while an operation is being executed. The set SFSEC value will be added to the synchronous prescaler counter. If the counter counts down, the clock will be delayed, and the delay time is determined by the following formula: Delay (seconds)=SFSEC/(SPSC+1) When it takes effect at the same time with ADD1SECEN, the advance clock will be added by a fraction of a second; the specific added value is determined by the following formula: Advance(seconds)=(1-(SFSEC/(SPSC+1))) Conduct write operation to this bit and RSFLG bit can be cleared. The software keeps running until RSFLG is set to 1 to ensure that the value of the shadow register is synchronized with the shift time.
30:15	Reserved		
31	ADD1SECEN	W	Add One Second Enable 0: Not added 1: The clock/calender increases by one second This bit can only be written; read this byte and it is always 0. Writing to this bit is invalid while an operation is being executed. When it takes effect at the same time with SFSEC, it can increase the value of the clock by several tenths of a second.

20.7.11 RTC timestamp time register (RTC_TSTIME)

This register is valid only when TSFLG of RTC_STS is set to 1. When TSFLG bit is reset, the content of this register will be cleared.

Offset address: 0x30

Power-on reset value: 0x0000 0000

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
3:0	SECU	R	Second Ones Unit in BCD Format Setup
6:4	SECT	R	Second Ten's Place Unit in BCD Format Setup
7	Reserved		
11:8	MINU	R	Minute Ones Unit in BCD Format Setup
14:12	MINT	R	Minute Ten's Place Unit in BCD Format Setup
15	Reserved		
19:16	HRU	R	Hour Ones Unit in BCD Format Setup
21:20	HRT	R	Hour Ten's Place Unit in BCD Format Setup
22	TIMEFCFG	R	Time Format Configure 0: AM or 24-hour system 1: PM
31:23	Reserved		

20.7.12 RTC timestamp date register (RTC_TSDATE)

This register is valid only when TSFLG bit of RTC_STS is set to 1. When TSFLG bit is reset, this register will be cleared.

Offset address: 0x34

Power-on reset value: 0x0000 0000

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
3:0	DAYU	R	Day Ones Unit in BCD Format Setup
5:4	DAYT	R	Day Ten's Place Unit in BCD Format Setup
7:6	Reserved		
11:8	MONU	R	Month Ones Unit in BCD Format Setup
12	MONT	R	Month Ten's Place Unit in BCD Format Setup
15:13	WEEKSEL	R	Week Day Units Select 000: Disable 001: Monday ... 111: Sunday
31:16	Reserved		

20.7.13 RTC timestamp subsecond register (RTC_TSSUBSEC)

This register is valid only when TSFLG bit of RTC_STS register is set to 1. When TSFLG bit is reset, the content of this register will be cleared.

Offset address: 0x38

Power-on reset value: 0x0000 0000

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
15:0	SUBSEC	R	Sub Second Value Setup When a timestamp event occurs, SUBSEC[15:0] is the value in synchronous prescaler counter.
31:16	Reserved		

20.7.14 RTC calibration register (RTC_CAL)

This register is in write protection state.

Offset address: 0x3C

Power-on reset value: 0x0000 0000

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
8:0	RECALF	R/W	Reduced Calibration Frequency Reduced calendar frequency: Shield RECALF pulses within 2^{20} RTCCLK pulses (32sec if the output frequency is 32768 Hz) and the calendar frequency will be reduced (the resolution is 0.9537 ppm). Increased calendar frequency: It takes effect at the same time with ICALFEN
12:9	Reserved		

Field	Name	R/W	Description
13	CAL16CFG	R/W	16 Second Calibration Cycle Period Configure When CAL16CFG is set to 1, 16-second calibration cycle is used, and it cannot be set to 1 at the same time with CAL8CFG bit. When CAL16CFG=1, RECALF[0] is always 0.
14	CAL8CFG	R/W	8 Second Calibration Cycle Period Configure When CAL8CFG is set to 1, 8-second calibration cycle is used, and it cannot be set to 1 at the same time with CAL16CFG bit. When CAL8CFG=1, RECALF[1:0] is always 00.
15	ICALFEN	R/W	Increase Calibration Frequency Enable 0: RTCCLK pulse is not increased 1: One RTCCLK pulse is increased (the frequency increases by 488.5 ppm) every 211 pulses It takes effect at the same time with RECALF, and when the resolution is high, the calender frequency will be reduced. If the input frequency is 32768Hz, the number of RTCCLK pulses added in the 32-second window is determined by the following formula: (512*ICALFEN)–RECALF。
31:16	Reserved		

20.7.15 RTC tamper and multiplexing configuration register (RTC_TACFG)

Offset address: 0x40

Power-on reset value: 0x0000 0000

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
1:0	Reserved		
2	TPIEN	R/W	Tamper Interrupt Enable 0: Disable 1: Enable
3	TP2EN	R/W	RTC_TAMP2 Input Detection Enable 0: Disable 1: Enable
4	TP2ALCFG	R/W	RTC_TAMP2 Input Active Level Configure When TPFCSEL!=00, this bit determines that RTC_TAMP2 will trigger a tamper detection event when the input maintains high/low level. 0: Low level 1: High level When TPFCSEL=00, this bit determines that RTC_TAMP2 triggers a tamper detection event on rising/falling edge 0: Rising edge 1: Falling edge
6:5	Reserved		
7	TPTSEN	R/W	Tamper Detection Event Timestamp Enable This bit determines whether the timestamp generated by the tamper detection event is saved 0: Not saved 1: Saved This bit is still valid when TSEN=0 for RTC_CTRL register.
10:8	TPSFSEL	R/W	Tamper Sampling Frequency Select These bits determine the sampling frequency of each input of RTC_TAMPx.

Field	Name	R/W	Description
			000：RTCCLK/32768 001：RTCCLK/16384 010：RTCCLK/8192 011：RTCCLK/4096 100：RTCCLK/2048 101：RTCCLK/1024 110：RTCCLK/512 111：RTCCLK/256
12:11	TPFCSEL	R/W	RTC_TAMPx Filter Count Select These bits detemine the number of sampling times after which the tamper event is activated on specific level (TAMP*TRG). TPFCSEL is valid for each input of RTC_TAMPx. 00: Activate the tamper event on the edge where RTC_TAMPx input is converted into valid level 01: Continuous sampling twice 10: Continuous sampling four 11: Continuous sampling eight
14:13	TPPRDUSEL	R/W	RTC_TAMPx Precharge Duration Select These bits determine the number of RTCCLK cycles which are enabled by pull-up resistor before sampling; which is valid in each input of RTC_TAMPx. 00：1 01：2 10：4 11：8
15	TPPUDIS	R/W	RTC_TAMPx Pull-up Function Disable This bit determines whether all RTC_TAMPx pins are precharged before sampling. 0: Enable (internal pull-up is enabled) 1: Disable
17:16	Reserved		
18	PC13VAL	R/W	RTC_ALARM Output Type/PC13 Value Configure When PC13 is used to output RTC_ALARM, this bit determines the output mode of RTC_ALARM: 0: Open-drain output 1: Push-pull output When all RTC multiplexing functions are disabled and PC13EN=1, this bit is used to set PC13 output value.
19	PC13EN	R/W	PC13 Mode Enable 0: PC13 is controlled by GPIO configuration register, and in standby mode, PC13 is floating. 1: When RTC multiplexing function is disabled, PC13 is forced to push-pull output mode.
20	PC14VAL	R/W	PC14 Output Value Setup Disable LSECLK and PC14EN=1, and this bit sets the output value of PC14.
21	PC14EN	R/W	PC14 Mode Enable 0: PC14 is controlled by GPIO configuration register, and in standby mode, PC14 is floating. 1: When LSECLK is disabled, PC14 is forced to push-pull output mode
22	PC15VAL	R/W	PC15 Output Value Setup Disable LSECLK and PC15EN=1, and this bit sets the output value of PC15.
23	PC15EN	R/W	PC15 Mode Enable

Field	Name	R/W	Description
			0: PC15 is controlled by GPIO configuration register, and in standby mode, PC15 is floating. 1: When LSECLK is disabled, PC15 is forced to push-pull output mode.
31:24	Reserved		

20.7.16 RTC alarm A subsecond register (RTC_ALRMASS)

This register can be written only when ALREN of RTC_CTRL register is reset or is in initialization mode.

This register is in write protection state.

Offset address: 0x44

Power-on reset value: 0x0000 0000

System reset: 0xXXXX XXXX

Field	Name	R/W	Description
14:0	SUBSEC	R/W	Sub Second Value Setup The subsecond value is compared with the value in the synchronous prescaler counter to determine whether to activate the alarm A, and only the bits from 0 to MASKSEL-1 are compared.
23:15	Reserved		
27:24	MASKSEL	R/W	Mask the Most-significant Bits Starting at This Bit Select 0000: Alarm A is not compared. The alarm is set when the second unit increases by 1 0001: When comparing with alarm A, SUBSEC[14:1] is not involved, and only SUBSEC[0] is involved 0010: When comparing with alarm A, SUBSEC[14:2] is not involved, and only SUBSEC[1:0] is involved 0011: When comparing with alarm A, SUBSEC[14:3] is not involved, and only SUBSEC[2:0] is involved ... 1100: When comparing with alarm A, SUBSEC[14:12] is not involved, and only SUBSEC[11:0] is involved 1101: When comparing with alarm A, SUBSEC[14:13] is not involved, and only SUBSEC[12:0] is involved 1110: When comparing with alarm A, SUBSEC[14] is not involved, and only SUBSEC[13:0] is involved 1111: When comparing the alarm A, 15 SUBSEC bits all take part in, and the alarm can be activated only when all of them match. The synchronous counter overrun bit (Bit 15) is never compared. This bit is not 0 only after shift operation.
31:28	Reserved		

21 Universal Synchronous/Asynchronous Transceiver (USART)

21.1 Full Name and Abbreviation Description of Terms

Table 63 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Clear to Send	CTS
Request to Send	RTS
Most Significant Bit	MSB
Least Significant Bit	LSB
Guard	GRD
Overrun	OVR

21.2 Introduction

USART (universal synchronous/asynchronous transceiver) is a serial communication device that can flexibly exchange full-duplex and half-duplex data with external devices, and meets the requirements of external devices for industry standard NRZ asynchronous serial data format. USART also provides a wide range of baud rate for selection and supports multiprocessor communication.

USART not only supports standard asynchronous transmission and receiving mode, but also supports synchronous one-way communication and hardware flow control mode. USART also supports DMA function to realize high-speed data communication.

21.3 Main Characteristics

（1） Full duplex asynchronous communication

（2） Single-line half-duplex communication

（3） NRZ standard format

（4） Characteristics of programmable serial port:
- Data bit: 8 bits or 9 bits
- Check bits: Even parity check, odd parity check, no check
- Support 1, 2 stop bits

（5） Check control
- Transmit the check bit
- Check the received data

（6） Select speed and clock tolerance with programmable 8 or 16-time oversampling rate

（7） Programmable high or low priority

（8） Independent transmitter and receiver enable bit

（9） Independent signal polarity control transmitter and receiver

（10） Switch TX/RX pin

（11） Support timeout detection

（12） Programmable baud rate generator, with the baud rate up to 6Mbits/s

（13） Automatic baud rate detection

（14） Multiprocessor communication:
- If the address does not match, it will enter the mute mode
- Wake up from mute mode through idle bus detection or address flag detection

（15） Synchronous transmission mode

（16） Support hardware flow control and RS485 driver enable

（17） DMA can be used for continuous communication

（18） State flag bit:
- Transmission detection flag: The transmit register is empty, the receive register is not empty, and transmission is completed
- Error detection flag: Overrun error, noise error, parity error, frame error

（19） Multiple interrupt sources:
- The transmit register is empty
- Transmission is completed
- CTS changed
- The receive register cannot be empty
- Overload error
- Bus idle
- Parity error
- Noise error
- Overrun error
- Frame error
- Address/Character match
- Failed to receive interrupt on time

21.4 Functional Description

Table 64 USART Pin Description

Pin	Type	Description
USART_RX	Input	Data receiving
USART_TX	Output I/O (single-line mode/smart card mode)	Data transmission When the transmitter is enabled and does not transmit data, the default is high
USART_CK	Output	Clock output
USART_nRTS	Input	Request to send in hardware flow control mode
USART_nCTS	Output	Clear to send in hardware flow control mode
USART_DE	Input	Drive enable activating external transmitter/receiver

21.4.1 Single-line Half-duplex Communication

HDEN bit of USART_CTRL3 register determines whether to enter the single-line half-duplex mode.

When USART enters single-line half-duplex mode:

- CLKEN bit of USART_CTRL2 register must be cleared.
- RX pin is disabled.
- TX pin should be configured as open-drain output and connected with RX pin inside the chip.
- Transmitting data and receiving data cannot be carried out at the same time. The data cannot be received before they are transmitted. If needing to receive data, enabling receiving can be turned on only after TXCFLG bit of USART_STS register is set to 1.
- If there is data conflict on the bus, software management is needed to allocate the communication process.

21.4.2 Select the clock source

The clock source must be selected by clock control system before USART is enabled

（1） The clock source is selected according to the transmission speed and the possibility of use of USART in low-power mode.

（2） The clock source frequency is f_{CK}.

- The range of communication speed is determined by the clock source. USART should be enabled before the clock source is selected.
- When USART adopts dual clock domain or wakes up the stop mode, PCLK, LSECLK, HSICLK or SYSCLK can be the clock source; otherwise, the clock source is PCLK.
- If LSECLK and LSICLK are selected as the clock source, USART can receive data even in low-power mode. And it can select according to the received data and wake-up mode, and wake up MCU when necessary, so that DMA can read the received data.
- The receiver realizes the data recovery of different oversampling technologies configured by users to distinguish valid incoming data and noises, which requires a trade-off between the maximum communication speed and noise/clock inaccuracy immunity.

21.4.3 Frame Format

The frame format of data frame is controlled by USART_CTRL1 register

- The character length is controlled by DBLCFG bit, and can be set to 8 or 9 bits
- The PCEN bit controls whether to turn on the check bit
- The PCFG bit controls the check bit is odd or even

Table 65 USART Frame Format

DBLCFG bit	PCEN bit	USART data frame
0	0	Start bit+8-bit data+stop bit
0	1	Start bit+7-bit data+odd-even parity check bit+stop bit
1	0	Start bit+9-bit data+stop bit
1	1	Start bit+8-bit data+odd-even parity check bit+stop bit

Configurable stop bit

Different stop bits can be configured by STOPCFG bit of USART_CTRL2 register.

- 1 stop bit: The default stop bit

- 2 stop bits: Used in normal mode, single-line mode and hardware flow control mode

Check bit

PCFG bit of USART_CTRL1 determines the parity check bit; when PCFG=0, it is even parity check, on the contrary, it is odd parity check.

- Even check: When the number of frame data and check bit '1' is even, the even check bit is 0; otherwise it is 1.
- Odd check: When the number of frame data and check bit '1' is even, the odd check bit is 1; otherwise it is 0.
- Check generation: When transmitting data, set PCEN bit of USART_CTRL1 register, and the check bit will replace the MSB bit of the data and be transmitted.
- Parity check:
  - If the parity check fails, PEFLG flag bit of USART_STS register will be set.
  - If the check control is enabled, corresponding interrupt will be triggered. Write 1 to PECLR bit of USART_INTFCLR register, and PEFLG flag bit can be cleared.

21.4.4 Transmitter

When TXEN bit of the register USART_CTRL1 is set, the transmit shift register will output data through TX pin and the corresponding clock pulses will be output through CK pin.

21.4.4.1 Character transmit

During transmitting period of USART, the least significant bit of the data will be moved out by TX pin first. In this mode, USART transmit register is composed of USARTx_TXDATA send data register and send shift register.

A data frame is composed of the start bit, character and stop bit, so there is a low-level start bit in front of each character; then there is a high-level stop bits the number of which is configurable.

Transmission configuration steps

（1） Decide the word length by setting DBLCFG bit of USART_CTRL1 register

（2） Decide the number of stop bits by setting STOPCFG bit of USART_CTRL2 register

（3） If multi-buffer communication is selected, DMA should be enabled in USART_CTRL3 register

（4） Set the baud rate of communication in USART_BR register

（5） Set UEN bit of USART_CTRL1 register to enable USART. Wait for TXBEFLG bit of USART_STS register to be set to 1

（6） Enable TXEN bit in USART_CTRL1 register, and transmit an idle frame

（7） Write data to USART_TXDATA register (if DMA is not enabled, repeat step 7 for each byte to be transmitted)

（8） Wait for TXCFLG position 1 of USART_STS register, indicating transmission completion

Note: TXEN bit cannot be reset during data transmission; otherwise, the data on TX pin will be destroyed, which is because if the baud rate generator stops counting, the data being transmitted will be lost.

21.4.4.2 Single-byte communication

TXBEFLG bit can be cleared by writing USART_TXDATA register. When the TXBEFLG bit is set by hardware, the shift register will receive the data transferred from the transmit data register, then the data will be transmitted, and the transmit data register will be cleared. The next data can be written in the data register without covering the previous data.

（1） If TXBEIEN in USART_CTRL1 register is set to 1, an interrupt will be generated.

（2） If USART is in the state of transmitting data, write to the data register to save the data to the TXDATA register, and transfer the data to the shift register at the end of the current data transmission.

（3） If USART is in idle state, write to the data register, put the data into the shift register, start transmitting data, and set TXBEFLG bit to 1.

（4） When a data transmission is completed and TXBEFLG bit is set, TXCFLG bit will be set to 1; at this time if TXCIEN bit in USART_CTRL1 register is set to 1, an interrupt will be generated.

（5） After the last data is written in the USART_TXDATA register, before entering the low-power mode or before closing the USART module, wait to set TXCFLG to 1.

21.4.4.3 Break frame

It is regarded that the break frames all receive '0' within one frame period. One break frame can be transmitted by setting TXBFQ bit of USART_REQUEST register, and the length of the break frame is determined by DBLCFG bit of USART_CTRL1 register. If the TXBFQ bit is set, after completion of transmission of current data, the TX line will transmit a break frame, and after completion of transmission of break frame, this bit will be reset. At the end of the break frame, the transmitter inserts 1 or 2 stop bits to respond to the start bit.

Note: If the TXBFQ bit is reset before transmission of the break frame starts, the break frame will not be transmitted. To transmit two consecutive break frames, the TXBFQ bit should be set after the stop bit of the previous break symbol.

21.4.4.4 Idle frame

The idle frame is regarded as a complete data frame composed entirely of '1', followed by the start bit of the next frame containing the data. Set TXEN bit of USART_CTRL1 register to 1 and one idle frame can be set before the first data frame.

21.4.5 Receiver

21.4.5.1 Character receive

During receiving period of USART, RX pin will first introduce the least significant bit of the data. In this mode, USART_RXDATA register has a buffer between the internal bus and the receive shift register. The data is transmitted to the buffer bit by bit. When fully receiving the data, the corresponding receive register is not empty, then the user can read USART_RXDATA.

Receiving configuration steps

（1） The programming oversampling rate is 8 or 16 times

（2） Decide the word length by setting DBLCFG bit of USART_CTRL1 register

（3） Decide the number of stop bits by setting STOPCFG bit of USART_CTRL2 register

（4） If multi-buffer communication is selected, DMA should be enabled in USART_CTRL3 register

（5） Set the baud rate of communication in USART_BR register

（6） Set UEN bit of USART_CTRL1 register to enable USART

（7） Set RXEN bit of USART_CTRL1 to enable receiving

Note:

（1）RXEN bit cannot be reset during data receiving period; otherwise, the bytes being received will be lost.

（2）In the process when the receiver is receiving a data frame, if overrun error, noise error or frame error is detected, the error flag will be set to 1.

（3）When data is transferred from the shift register to USART_RXDATA register, the RXBNEFLG bit of USART_STS will be set by hardware.

（4）An interrupt will be generated if RXBNEIEN bit is set.

（5）In single buffer mode, the RXBNEFLG bit can be cleared by reading USART_RXDATA register by software or by writing 0.

（6）In multi-buffer mode, after each byte is received, RXBNEFLG bit of USART_STS register will be set to 1, and DMA will read the data register to clear it.

21.4.5.2 Break frame

When the receiver receives a break frame, USART will handle it as receiving a frame error.

21.4.5.3 Idle frame

When the receiver receives an idle frame, USART will handle it as receiving an ordinary data frame; if IDLEIEN bit of USART_CTRL1 is set, an interrupt will be generated.

21.4.5.4 Oversampling rate

OSMCFG bit of USART_CTRL1 register determines the oversampling rate.

If the oversampling rate is 8 times of the baud rate, the speed is higher, but the clock tolerance is smaller. If it is 16 times, the speed is lower, but the clock tolerance is bigger.

21.4.5.5 Overrun error

When RXBNEFLG bit of USART_STS register is set to 1 and a new character is received at the same time, an overrun error will be caused. Only after RXEN is reset, can the data be transferred from the shift register to RXDATA register. RXBNEFLG bit will be set to 1 after receiving the byte. This bit needs to be reset before receiving the next data or serving the previous DMA request; otherwise, an overrun error will be caused.

When an overrun error occurs

- OVREFLG bit of USART_STS is set to 1
- The data in RXDATA register will not be lost
- The data in the shift register received before will be overwritten, but the data received later will not be saved
- If RXBNEIEN bit or ERRIEN bit of USART_CTRL1 is set, an interrupt will be generated
- When OVREFLG bit is set, it means there are data lost. There are two possibilities:
  - When RXBNEFLG=1, the previous valid data is still on RXDATA register, and can be read
  - When RXBNEFLG=0, there is no valid data in RXDATA register.
- The OVREFLG bit can be reset through read operation for USART_STS and USART_RXDATA registers.

21.4.5.6 Noise error

When noise is detected in receiving process of the receiver:

- Set NEFLG flag on the rising edge of RXBNEFLG bit of USART_STS register
- Invalid data is transmitted from the shift register to USART_RXDATA register.
- In single byte communication, there is no interrupt, but in multi-buffer communication, an interrupt will be generated by setting the ERRIEN bit of USART_CTRL3 register

21.4.5.7 Frame error

If the stop bit is not received and recognized at the expected receiving time due to excessive noise or lack of synchronization, a frame error will be detected.

When a frame error is detected in receiving process of the receiver:

- Set the FEFLG bit of USART_STS register
- Invalid data is transmitted from the shift register to USART_RXDATA register.
- In single byte communication, there is no interrupt, but in multi-buffer communication, an interrupt will be generated by setting the ERRIEN bit of USART_CTRL3 register

21.4.6 Tolerance of Receiver to the Change of Clock

Only when the total clock system deviation is less than the tolerance of USART receiver, can the USART receiver work normally.

Deviation will occur in any of the following circumstances:

（1） DTRA: Deviation caused by transmitter error

（2） DQUANT: Deviation caused by receiver baud rate quantization

（3） DREC: Change of receiver oscillator

（4） DTCL: Deviation caused by transmission line

21.4.7 Baud Rate Generator

The baud rate division factor (USARTDIV) is a 16-digit number consisting of 12-digit integer part and 4-digit decimal part.

When the configuration is 16x oversampling (that is, OSMCFG=0 of the

USARTx_CTRL1 register), the formula for calculating the baud rate is as follows:

$$\text{Baud rate} = \frac{f_{CK}}{USARTDIV}$$

When the configuration is 8x oversampling (that is, OSMCFG=1 of the USARTx_CTRL1 register), the formula for calculating the baud rate is as follows:

$$\text{Baud rate} = \frac{2 \times f_{CK}}{USARTDIV}$$

Note:

（1）The value of f_{CK} is PCLK, where the peripheral clock of USART2 is PCLK1; The peripheral clock of USART1 needs to be determined by referring to the value selection of USART1SEL in the RCM_CFG3 register, and PCLK is PCLK2.

（2）USARTDIV is the unsigned decimal value of the USARTx_BR register; However, when OSMCFG=1, the value of USARTDIV[3:0] is shifted one bit to the right while keeping USARTDIV[3]=0. USART can be enabled only after the clock control unit enables the system clock.

21.4.8 Automatic Baud Rate Detection

When a character is received, USART can detect and automatically set the value of the USART_BR register. Automatic baud rate detection is conducted when the communication speed of the system is unknown, when the clock source with low precision is used, or when the clock deviation is not measured to obtain the correct bit rate. The clock source must be compatible with the expected communication speed.

A non-zero baud rate must be written for initialization; confirm the character content, and then turn on automatic baud rate detection. ABRDCFG bit of USART_CTRL2 register can be set to select the character content, and the possible character content is:

（1） For all bit starting with 1, in this case, measure the length of the start bit (the duration from the falling edge to the rising edge).

（2） For all bit starting with 10xx, in this case, measure the length of the start bit and the first data bit, the duration of the falling edge, to ensure better accuracy when the signal slew rate is small.

ABRDEN bit of USART_CTRL2 register determines whether to turn on automatic baud rate detection. After the automatic baud rate detection is turned on, wait for the first character on RX line. After detection, ABRDFLG flag bit of USART_STS register will be set.

Note:

（1）If the line noise is too high, correct baud rate cannot be guaranteed. In this case, the BR value may be damaged and the ABRDEFLG flag bit will be set. This situation can also happen if the communication speed and automatic baud rate detection is not compatible.

（2）RXBNEFLG interrupt will be generated after detection.

（3）At any time, automatic baud rate detection may be restarted by resetting the ABRDFLG flag (writing a 0).

（4）USART cannot be disabled during automatic baud rate detection; otherwise, the BR value may be damaged.

21.4.9 Multi-processor Communication

In multi-processor communication, multiple USARTs are connected to form a network. In this network, two devices communicate with each other, and the mute mode can be enabled for other devices not participating in the communication in order to reduce the burden of USART. In mute mode, no receive state bit will be set, and all receive interrupts are disabled.

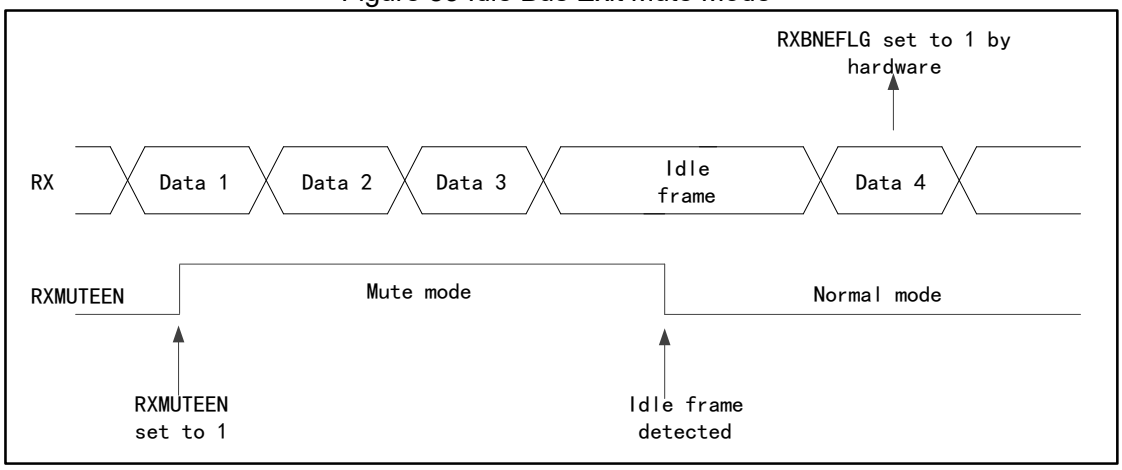
When mute mode is enabled, there are two ways to exit the mute mode:

- WUPMCFG bit is cleared and the bus is idle to exit the mute mode.
- WUPMCFG bit is set and after receiving the address flag, it can exit the mute mode.

Idle bus detection (WUPMCFG=0)

When RXMUTEEN is set to 1, USART enters the mute mode, and it can be waken up from the mute mode when an idle frame is detected, meanwhile, the RXMUTEEN bit will be cleared by the hardware. RXMUTEEN can also be cleared by software.

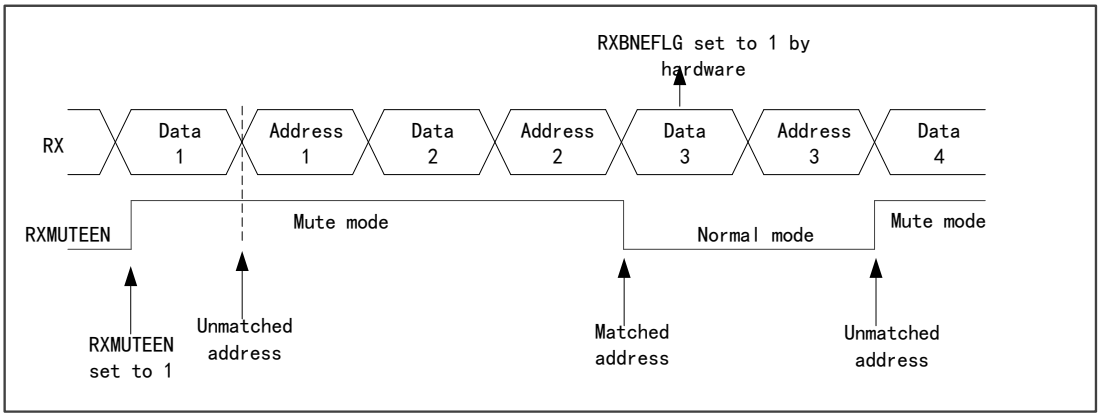
Figure 83 Idle Bus Exit Mute Mode



Address flag detection (WUPMCFG=1)

If the address flag bit is 1, this byte is regarded as the address. The storage address of lower four bits of the address bytes will first be compared with its own address when the receiver receives the address byte. If the addresses do not match, the receiver will enter the mute mode. If the addresses match, the receiver will wake up from the mute mode and be ready to receive the next byte. If the address byte is received again after exiting the mute mode, but the address does not match its own address, the receiver will enter the mute mode again.

Figure 84 Address Flag Exit Mute Mode



21.4.10 Synchronous Mode

The synchronous mode supports full duplex synchronous serial communication in master mode, and has one more signal line USART_CK which can output synchronous clock than the asynchronous mode.

CLKEN bit of USART_CTRL2 register decides whether to enter the synchronous mode.

When USART enters the synchronous mode:

- HDEN bit of USART_CTRL3 register must be cleared
- The start bit and stop bit of the data frame have no clock output
- Whether the last data bit of the data frame generates USART_CK clock is determined by LBCPOEN bit of the register USART_CTRL2
- The clock polarity of USART_CK is decided by CPOL bit of USART_CTRL2 register
- The phase of USART_CK is decided by the CPHA bit of USART_CTRL2
- The external CK clock cannot be activated when the bus is idle or the frame is disconnected

Figure 85 USART Synchronous Transmission Example

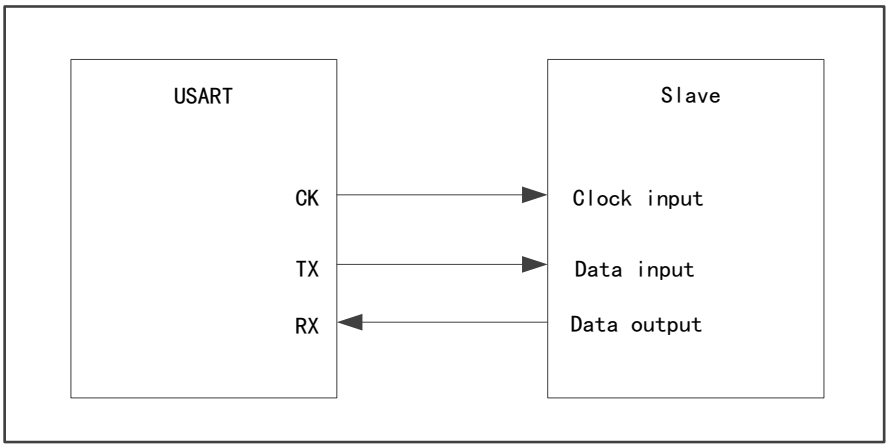


Figure 97 USART Synchronous Transmission Timing Diagram (DBLCFG=10)

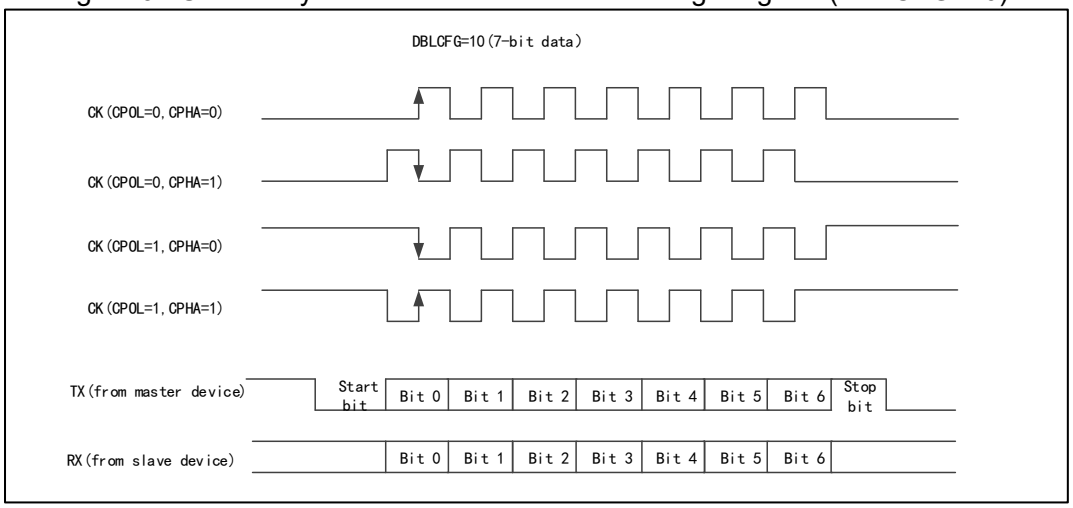


Figure 86 USART Synchronous Transmission Timing Diagram (DBLCFG0=0)

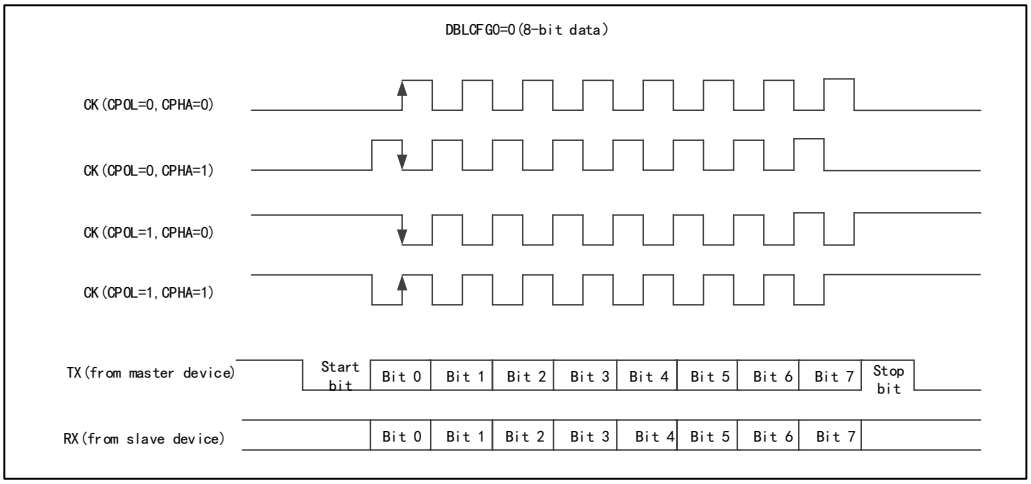
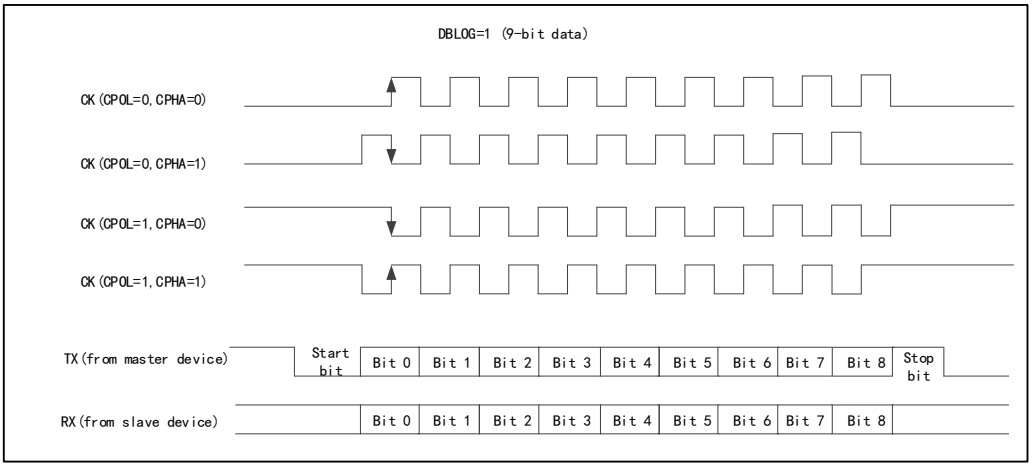


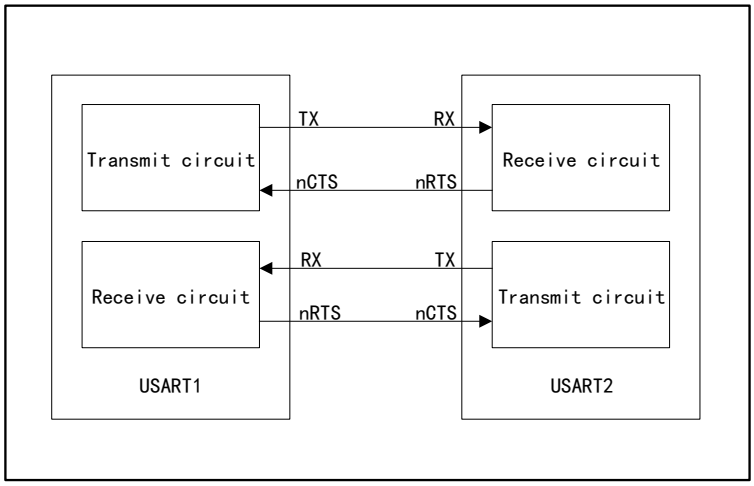
Figure 87 USART Synchronous Transmission Timing Diagram (DBLCFG=1)



21.4.11 Hardware Flow Control and RS485 Drive Enable

The function of hardware flow control is to control the serial data flow between two devices through nCTS pin and nRTS pin.

Figure 88 Hardware Flow Control between Two USARTs



CTS flow control

CTSEN bit of USART_CTRL3 register determines whether CTS flow control is enabled. If CTS flow control is enabled, the transmitter will detect whether the data frame of nCTS pin can be transmitted. If TXBEFLG bit=0 for USART_STS register and nCTS is pulled to low level, the data frame can be transmitted. If nCTS becomes high during transmission, the transmitter will stop transmitting after the current data frame is transmitted.

RTS flow control

RTSEN bit of USART_CTRL3 register determines whether RTS flow control is enabled. If RTS flow control is enabled, when the receiver receives data, nRTS will be pulled to low level. When a data frame is received, nRTS will becomes high to inform the transmitter to stop transmitting data frame.

RS485 driver enable

DEN bit of USART_CTRL3 register determines whether to turn on the driver enable function, and this function can allow DE signal to turn on the control terminal of the external transceiver.

Lead time: The time interval between the driver enable signal and the start bit of the first byte. Controlled by DLTEN[4:0] of USART_CTRL1 controller.

Lag time: The time interval between the stop bit of the last byte and the release DE signal. Controlled by DDLTEN[4:0] of USART_CTRL1 register.

21.4.12 DMA Multi-processor Communication

USART can access the data buffer in DMA mode in order to reduce the burden of processors.

Transmission in DMA mode

DMATXEN bit of USART_CTRL3 register determines whether to transmit in DMA mode. When transmitting by DMA, the data in the designated SRAM will be transmitted to the buffer by DMA.

Configuration steps of transmission by DMA:

（1） Clear the TXCFLG flag bit of USART_STS register

（2） Set the address of SRAM memory storing data as DMA source address

（3） Set the address of USART_TXDATA register as DMA destination address

（4） Set the number of data bytes to be transmitted

（5） Set channel priority

（6） Set interrupt enable

（7） Enable DMA channel

（8） Wait for TXCFLG position 1 of USART_STS register, indicating transmission completion

Receive in DMA mode

DMARXEN bit of USART_CTRL3 register determines whether to receive by DMA. When receiving by DMA, every time one byte is received, the data in the receive buffer will be transmitted to the designated SRAM area by DMA.

Configuration steps of receiving by DMA:

（1） Set the address of USART_RXDATA register as DMA source address

（2） Set the address of SRAM memory storing data as DMA destination address

（3） Set the number of data bytes to be transmitted

（4） Set channel priority

（5） Set interrupt enable

（6） Enable DMA channel

21.4.13 Interrupt Request

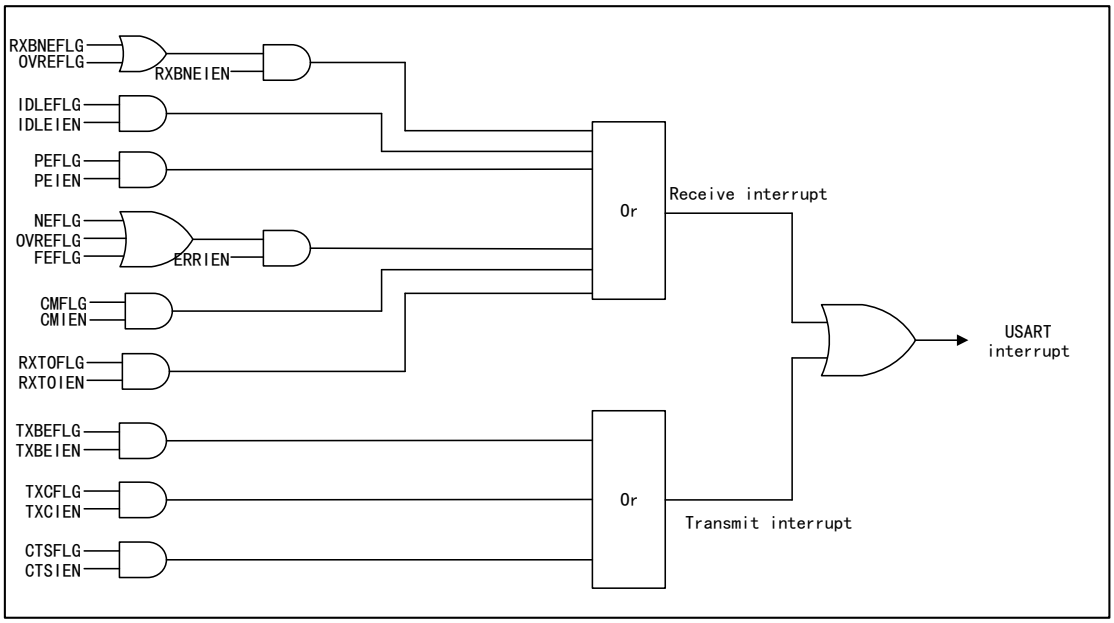
Table 66 USART Interrupt Request

Interrupt event		Event flag bit	Enable bit
The receive register cannot be empty		RXBNEFLG	RXBNEIEN
Overload error		OVREFLG	
Line idle is detected		IDLEFLG	IDLEIEN
Odd-even parity error		PEFLG	PEIEN
Receiving error in DMA mode	Noise error	NEFLG	ERRIEN
	Overrun error	OVREFLG	
	Frame error	FEFLG	
Matching character		CMFLG	CMIEN

Interrupt event	Event flag bit	Enable bit
Error of failing to receive on time	RXTOFLG	RXTOIEN
Transmit data register is empty	TXBEFLG	TXBEIEN
Transmission is completed	TXCFLG	TXCIEN
CTS flag	CTSFLG	CTSIEN

All interrupt requests of USART are connected to the same interrupt controller, and the interrupt requests have logical or relational before they are transmitted to the interrupt controller.

Figure 89 USART Interrupt Mapping



21.4.14 Comparison of USART Supporting Functions

Table 67 Comparison of USART Supporting Functions

USART mode	USART1	USART2
Hardware flow control	√	√
Multi-buffer communication (DMA)	√	√
Multi-processor communication	√	√
Synchronous	√	√
Half duplex (single-line mode)	√	√
Receiving timeout interrupt	√	√
Support the automatic baud rate detection mode	2	4

Note:

（1）"√" means this function is supported, while "—" means that this function is not supported.

（2）Receiver timeout interrupt and USART2 and USART3 supporting automatic baud rate detection are supported only by APM32F030xC.

（3）APM32F030x4x6x8 A version of the chip K6U6,K6T6,K8T6,C6T6,C6T6 only USART1, while the B version has two USART, other configurations are consistent.

21.5 Register Address Mapping

Table 68 USART Register Address Mapping

Register name	Description	Offset address
USART_CTRL1	Control register 1	0x00
USART_CTRL2	Control register 2	0x04
USART_CTRL3	Control register 3	0x08
USART_BR	Baud rate register	0x0C
USART_RXTO	Receive timeout register	0x14
USART_REQUEST	Request register	0x18
USART_STS	Interrupt and state register	0x1C
USART_INTFCLR	Interrupt flag clear register	0x20
USART_RXDATA	Receive data register	0x24
USART_TXDATA	Transmit data register	0x28

21.6 Register Functional Description

21.6.1 Control register 1 (USART_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	UEN	R/W	USART Enable 0: USART frequency divider and output are disabled 1: USART module is enabled Set 1 or clear 0 by software; clearing this bit will cancel the current operation and the prescaler and output of USART will stop working immediately. The setting for USART will not be reset, but the state flag in USART_STS will be reset.
1	Reserved		
2	RXEN	R/W	Receive Enable 0: Disable 1: Enable, and start to detect the start bit on RX pin Set 1 or clear 0 by software.
3	TXEN	R/W	Transmitte Enable 0: Disable 1: Enable Set 1 or clear 0 by software.
4	IDLEIEN	R/W	IDLE Interrupt Enable 0: Disable 1: Generate an interrupt when IDLEFLG is set Set 1 or clear 0 by software.

Field	Name	R/W	Description
5	RXBNEIEN	R/W	Receive Buffer Not Empty Interrupt Enable 0: Disable 1: Generate an interrupt when OVREFLG or RXBNEFLG is set Set 1 or clear 0 by software.
6	TXCIEN	R/W	Transmit Complete Interrupt Enable 0: Disable 1: Generate an interrupt when TXCFLG is set Set 1 or clear 0 by software.
7	TXBEIEN	R/W	Transmit Buffer Empty Interrupt Enable 0: Disable 1: Generate an interrupt when TXBEFLG is set Set 1 or clear 0 by software.
8	PEIEN	R/W	Parity Error interrupt Enable 0: Disable 1: Generate an interrupt when PEFLG is set Set 1 or clear 0 by software.
9	PCFG	R/W	Odd/Even Parity Configure 0: Even parity check 1: Odd parity check Set 1 or clear 0 by software. This bit can be set only when USART is not enabled.
10	PCEN	R/W	Parity Control Enable 0: Disable 1: Enable If this bit is set, a check bit will be inserted in the most significant bit when transmitting data; when receiving data, check whether the check bit of the received data is correct. This bit can be set only when USART is not enabled.
11	WUPMCFG	R/W	Wakeup Method Configure 0: Idle bus wakeup 1: Address tag wakeup Set 1 or clear 0 by software. This bit can be set only when USART is not enabled.
12	DBLCFG0	R/W	Data Bits Length Configure 0: 1 start bit, 8 data bits, n stop bits 1: 1 start bit, 9 data bits, n stop bits Set 1 or clear 0 by software. This bit cannot be modified during transmission of data.
13	RXMUTEEN	R/W	Receive Mute Mode Enable 0: Normal working mode 1: Can switch between normal mode and mute mode Set 1 or clear 0 by software.
14	CMIEN	R/W	Character Match Interrupt Enable 0: Disable 1: Generate an interrupt when CMFLG is set Set 1 or clear 0 by software.
15	OSMCFG	R/W	Oversampling Mode Configure 0: 16-time oversampling 1: 8-time oversampling This bit can be set only when USART is not enabled.
20:16	DDLTEN[4:0]	R/W	Driver De-lead Time Enable This bit field is the time interval between the last stop bit and DE signal during transmission. Its unit is sampling time, determined by oversampling rate. If write operation is performed for USART_TXDATA within DDLTEN

Field	Name	R/W	Description
			time, the just written data will be transmitted only after DDLTEN and DLTEN time. This bit field can be set only when USART is not enabled.
25:21	DLTEN[4:0]	R/W	Driver Lead Time Enable This bit field is the time interval between DE signal and the first start bit during transmission. Its unit is sampling time, determined by oversampling rate. This bit field can be set only when USART is not enabled.
26	RXTOIEN	R/W	Receiver Timeout Interrupt Enable 0: Disable 1: Generate an interrupt when RXTOFLG is set Set or cleared by software.
31:27	Reserved		

21.6.2 Control register 2 (USART_CTRL2)

Offset address: 0x04

Reset value: 0x0000

Field	Name	R/W	Description
3:0	Reserved		
4	ADDRLEN	R/W	Slave Address Length Configure 0: 4-bit address 1: 7-bit address This bit field can be set only when USART is not enabled.
7:5	Reserved		
8	LBCPOEN	R/W	Last Bit Clock Pulse Output Enable 0: Not output from CK 1: Output from CK This bit is valid only in synchronous mode.
9	CPHA	R/W	Clock Phase Configure This bit indicates on the edge of which clock sampling is conducted 0: The first 1: The second This bit is valid only in synchronous mode. This bit can be set only when USART is not enabled.
10	CPOL	R/W	Clock Polarity Configure The state of CK pin when USART is in idle state 0: Low level 1: High level This bit is valid only in synchronous mode. This bit can be set only when USART is not enabled.
11	CLKEN	R/W	Clock Enable (CK pin) 0: Disable 1: Enable This bit can be set only when USART is not enabled.
13:12	STOPCFG	R/W	STOP Bit Configure 00: 1 stop bit 01: Reserved 10: 2 stop bits 11: Reserved This bit can be set only when USART is not enabled.

Field	Name	R/W	Description
14	Reserved		
15	SWAPEN	R/W	Swap TX/RX Pins Function Enable 0: Use according to standard allocation 1: The functions of TX and RX pins can be exchanged for use, and they will work when crossing and interconnecting with other USART. Set or cleared by software. This bit can be set only when USART is not enabled.
16	RXINVEN	R/W	RX Pin Active Level Inversion Enable 0: Standard logic level (V_{DD} =1/IDLE, Gnd=0/mark) 1: Reverse direction (V_{DD} =0/mark, Gnd=1/IDLE), which works when there is an external phase inverter on RX line. Set or cleared by software. This bit can be set only when USART is not enabled.
17	TXINVEN	R/W	TX Pin Active Level Inversion Enable 0: Standard logic level (V_{DD} =1/IDLE, Gnd=0/mark) 1: Reverse direction (V_{DD} =0/mark, Gnd=1/IDLE), which works when there is an external phase inverter on TX line. Set or cleared by software. This bit can be set only when USART is not enabled.
18	BINVEN	R/W	Binary Data Inversion Enable 0: Positive/Direct logic (0=L, 1=H) 1: Negative/Reverse logic (0=H, 1=L) Set or cleared by software. This bit can be set only when USART is not enabled. The check bit will be inverted when this bit is set.
19	MSBFEN	R/W	Most Significant Bit First Enable 0: The data of No. 0 bit immediately follows the start bit 1: The data of the most significant bit immediately follows the start bit Set or cleared by software. This bit can be set only when USART is not enabled.
20	ABRDEN	R/W	Auto Baud Rate Detection Enable 0: Disable 1: Enable Set or cleared by software.
22:21	ABRDCFG	R/W	Auto Baud Rate Detection Mode Configure 00: Measure the start bit 01: Measure the falling edge 10: 0x7F frame detection 11: 0x55 frame detection Set or cleared by software.
23	RXTODEN	R/W	Receive Timeout Detection Function Enable 0: Disable 1: Enable Set or cleared by software. Set this bit, and when it is detected that the RX line is idle for the length of time configured by RXTO register, the RXTOFLG bit will be set by hardware.
27:24	ADDRL	R/W	USART Device Node Address Low Setup

Field	Name	R/W	Description
			This bit field is used for wake-up detection of 7-bit address flag which is used for multi-computer communication and enters the mute state or stop mode. This bit can be set only when the receiver is turned off or USAR is not enabled.
31:28	ADDRH	R/W	USART Device Node Address High Setup This bit field is not only used for wake-up detection of 7-bit address flag which is used for multi-computer communication and enters the mute state or stop mode. (The most significant bit of the character of the transmitter should be 1) But is also used for character detection in normal receiving process. (Then the mute state is disabled) Then if the received 8-bit byte matches ADDRH, CMFLG bit will be set. This bit can be set only when the receiver is turned off or USAR is not enabled.

21.6.3 Control register 3 (USART_CTRL3)

Offset address: 0x08

Reset value: 0x0000

Field	Name	R/W	Description
0	ERRIEN	R/W	Error interrupt Enable 0: Disable 1: Enabled; when any bit among FEFLG, OVREFLG and NEFLG is set, an interrupt will be generated.
2:1	Reserved		
3	HDEN	R/W	Half-duplex Mode Enable 0: Disable 1: Enable This bit can be set only when USART is not enabled.
5:4	Reserved		
6	DMARXEN	R/W	DMA Receive Enable 0: Disable 1: Enable Set or cleared by software.
7	DMATXEN	R/W	DMA Transmit Enable 0: Disable 1: Enable Set or cleared by software.
8	RTSEN	R/W	RTS Hardware Flow Control Function Enable 0: Disable 1: Enable RTS: Require To Send, which is output signal, indicating it has been ready to receive. Request is made to receive data only when there is space in the receive buffer; when data can be received, RTS output is pulled to low level. This bit can be set only when USART is not enabled.
9	CTSEN	R/W	CTS Function Enable 0: Disable 1: Enable CTS: Clear To Send, which is input signal

Field	Name	R/W	Description
			When CTS input signal is at low level, the data can be transmitted; otherwise, the data cannot be transmitted; if CTS signal is pulled to high during data transmission, the data transmission will be stopped after the data transmission is completed; if write operation is performed for the data register when CTS is high, the data will not be transmitted until CTS is valid. This bit can be set only when USART is not enabled.
10	CTSIEN	R/W	CTS Interrupt Enable 0: Disable 1: Generate an interrupt when CTSFLG is set
11	SAMCFG	R/W	Sample Method Configure 0: Sampling for three times 1: Single sample; flag of noise detection disabled This bit can be set only when USART is not enabled.
12	OVRDEDIS	R/W	Overrun Detection Disable 0: Enable. When RXBNEFLG bit is set and new data is received, OVREFLG bit will be set. 1: Disable. When new data are received, if RXBNEFLG is still set but OVREFLG is not set, the data not read will be covered by new data. This bit can be set only when USART is not enabled.
13	DDISRXEEN	R/W	DMA Disable on Receive Error Enable 0: DMA not disabled. The corresponding error flag bit will be set, but in order to avoid data from overrunning and being covered, RXBNEFLG will not be set. In smart card mode, as a result, no DMA request will be issued, so wrong data will not be transmitted, but the next correct data will be transmitted. 1: DMA disabled. If RXBNEFLG is set, the corresponding error flag bit will also be set. DMA request will not be masked only when the corresponding error flag bit is cleared. Therefore, it is required to first disable DMA request or first clear RXBNEFLG flag and then clear the error flag. This bit can be set only when USART is not enabled.
14	DEN	R/W	Driver Enable Users are allowed to activate the control terminal of external transceiver through DE signal. 0: DE function disabled 1: DE function enabled, DE signal output on RTS pin This bit can be set only when USART is not enabled.
15	DPCFG	R/W	Driver Polarity Configure 0: DE signal high level is valid 1: DE signal low level is valid This bit can be set only when USART is not enabled.
31:16	Reserved		

21.6.4 Baud rate register (USART_BR)

This register can be set only when USART is not enabled. This bit may be reset by hardware during automatic baud rate detection.

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
3:0	FBR	R/W	Fraction of USART Baud Rate Divider factor

Field	Name	R/W	Description
			The decimal part of USART baud rate division factor USARTDIV[3:0] is determined by these four bits.
15:4	IBR	R/W	Integer of USART Baud Rate Divider factor The integral part of USART baud rate division factor USARTDIV[15:4] is determined by these 12 bits.
31:16	Reserved		

21.6.5 Receive timeout register (USART_RXTO)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
23:0	RXTO	R/W	Receiver Timeout Value Setup This bit field specifies the receive timeout value in baud clock. In standard mode, after the last byte is received, if no new start bit is detected within the duration of RXTO value, RXTOFLG will be set by hardware.
31:24	Reserved		

21.6.6 Request register (USART_REQUEST)

Offset address: 0x18

Reset value: 0x0000

Field	Name	R/W	Description
0	ABRDQ	W	Auto Baud Rate Detection Request Set this bit, the ABRDFLG flag will be cleared and an automatic baud rate detection will be conducted when the data is received next time.
1	TXBFQ	W	Transmit Break Frame Request Set this bit, TXBFFLG flag will be set and a break frame will be transmitted after the transmission state machine is enabled.
2	MUTEQ	W	Mute Mode Request Set this bit to enter the mute mode and RXWFMUTE flag will be cleared.
3	RXDFQ	W	Receive Data Flush Request Set this bit and RXBNEFLG flag will be cleared. The data that has not been read out in the receive register can be discarded to avoid overrun error.
31:4	Reserved		

21.6.7 Interrupt and state register (USART_STS)

Offset address: 0x1C

Reset value: 0x0200 00C0

Field	Name	R/W	Description
0	PEFLG	R	Parity Error Occur Flag 0: No error 1: Parity error is detected In receiving mode, when a parity error occurs, it is set to 1 by hardware; set PECLR and this bit can be cleared.
1	FEFLG	R	Frame Error Occur Flag 0: No frame error 1: Frame error or break symbol is detected

Field	Name	R/W	Description
			When there is synchronous dislocation, too much noise or break symbol, this bit is set to 1 by hardware; set FECLR and this bit can be cleared.
2	NEFLG	R	Noise Error Occur Flag 0: No noise 1: Noise is detected When there is noise error, this bit is set to 1 by hardware; set NFCLR and this bit can be cleared.
3	OVREFLG	R	Overrun Error Occur Flag 0: No overrun error 1: Overrun error is detected When the RXBNEFLG bit is set and the data in the shift register is to be transmitted to the receive register, set to 1 by hardware; set OVRECLR and this bit can be cleared.
4	IDLEFLG	R	IDLE Line Detected Flag 0: Idle bus is not detected 1: Idle bus is detected When idle bus is detected, this bit is set to 1 by hardware; this bit can be cleared by setting IDLECLR.
5	RXBNEFLG	R	Receive Data Buffer Not Empty Flag 0: The receive data buffer is empty 1: The receive data buffer is not empty When the data register receives the data transmitted by the receive shift register, it is set to 1 by hardware; this bit can be cleared by reading the TXDATA register or setting RXDFQ.
6	TXCFLG	R	Transmit Data Complete Flag 0: Transmit data is not completed 1: Transmit data is completed After the last frame of data is transmitted and the TXBEFLG is set, set to 1 by hardware; conduct write operation to TXDATA register or set TXCCLR and this bit can be cleared.
7	TXBEFLG	R	Transmit Data Buffer Empty Flag 0: The transmit data buffer is not empty 1: The transmit data buffer is empty When the shift register receives the data transmitted by the transmit data register, this bit is set to 1 by hardware; this bit can be cleared by performing write operation on TXDATA register.
8	Reserved		
9	CTSFLG	R	CTS Change Flag 0: No change on nCTS state line 1: There is change on nCTS state line If the CTSEN bit is set, when switching to the nCTS input, set to 1 by hardware; this bit can be cleared by setting CTSCLR.
10	CTSCFG	R	CTS Status Configure 0: Set nCTS line 1: Reset nCTS line This bit set 1 or clear 0 by hardware. This bit sets reversed state of nCTS input pin.
11	RXTOFLG	R	Receiver Timeout Flag 0: No timeout 1: Timed out If the start bit is not detected within the duration set by RXTO bit, this bit is set to 1 by hardware; this bit can be cleared by setting RXTOCLR bit.

Field	Name	R/W	Description
13:12	Reserved		
14	ABRDEFLG	R	Auto Baud Rate Detection Error Flag This bit is set to 1 by hardware when baud rate detection fails; this bit can be cleared by setting ABRDQ bit. 0: No automatic baud rate detection error occurred 1: Automatic baud rate detection error occurred
15	ABRDFLG	R	Auto Baud Rate Detection Flag When the automatic baud rate function is turned on or when the automatic baud rate operation is interrupted, it is set to 1 by hardware; this bit is cleared when resuming the baud rate detection. 0: Automatic baud rate detection is not performed 1: Automatic baud rate detection complete
16	BSYFLG	R	Busy Flag 0: Idle state 1: In the process of receiving data This bit is set to 1 by hardware when the start bit is detected, and it will be cleared after receiving is over. This bit set 1 or clear 0 by hardware.
17	CMFLG	R	Character Match Flag 0: No character matches 1: There is matching character When the received character matches the value set by ADDR[7:0], this bit is set to 1 by hardware; this bit can be cleared by setting CMCLR bit.
18	TXBFFLG	R	Transmit Break Frame Flag 0: Not transmit 1: Will transmit If TXBFQ bit is set, this bit can be set to 1 by software; when transmitting the stop bit of the break frame, this bit is cleared by hardware.
19	RXWFMUTE	R	Receiver Wakeup From Mute Mode 0: Normal mode 1: Mute mode When switching the wake-up mode and the mute mode, this bit shall be set to 1 and cleared by hardware; if it is waken up by idle signal, this bit can be set to 1 by writing to USART_REQUEST register. WUPMCFG bit determines the control sequence of mute mode.
31:20	Reserved		

21.6.8 Interrupt flag clear register (USART_INTFCLR)

Offset address: 0x20

Reset value: 0x0000

Field	Name	R/W	Description
0	PECLR	RC_W1	Parity Error Flag Clear Set this bit and PEFLG flag bit of USART_STS register can be cleared. 0: Invalid operation 1: Clear PEFLG
1	FECLR	RC_W1	Framing Error Flag Clear Set this bit and FEFLG flag bit of USART_STS register can be cleared. 0: Invalid operation 1: Clear FEFLG

Field	Name	R/W	Description
2	NECLR	RC_W1	Noise Detected Flag Clear Set this bit and NEFLG flag bit of USART_STS register can be cleared. 0: Invalid operation 1: Clear NEFLG
3	OVRECLR	RC_W1	Overrun Error Flag Clear Set this bit and OVREFLG flag bit of USART_STS register can be cleared. 0: Invalid operation 1: Clear OVREFLG
4	IDLECLR	RC_W1	IDLE Line Detected Clear Flag Set this bit and IDLEFLG flag bit of USART_STS register can be cleared. 0: Invalid operation 1: Clear IDELFLG
5	Reserved		
6	TXCCLR	RC_W1	Transmission Data Complete Flag Clear Set this bit and TXCFLG flag bit of USART_STS register can be cleared. 0: Invalid operation 1: Clear TXCFLG
8:7	Reserved		
9	CTSCLR	RC_W1	CTS Flag Clear Set this bit and CTSFLG flag bit of USART_STS register can be cleared. 0: Invalid operation 1: Clear CTSFLG
10	Reserved		
11	RXTOCLR	RC_W1	Receiver Timeout Flag Clear Set this bit and RXTOFLG flag bit of USART_STS register can be cleared. 0: Invalid operation 1: Clear RXTOFLG
16:12	Reserved		
17	CMCLR	RC_W1	Character Match Flag Clear Set this bit and CMFLG flag bit of USART_STS register can be cleared. 0: Invalid operation 1: Clear CMFLG
31:18	Reserved		

21.6.9 Receive data register (USART_RXDATA)

Offset address: 0x24

Reset value: 0xXXXX

Field	Name	R/W	Description
8:0	RXDATA	R	Receive Data Value Setup Transmit or receive data values; Data is read from it when it is received and written to it when it is sent.

Field	Name	R/W	Description
			If the parity bit is enabled, if there are 9 data bits, the 8th bit of data is the check bit. If there are 8 data bits, the 7th bit of data is the parity bit.
31:9	Reserved		

21.6.10 Transmit data register (USART_TXDATA)

Offset address: 0x28

Reset value: 0xXXXX

Field	Name	R/W	Description
8:0	TXDATA	R/W	Transmit Data Value Setup Include the data byte to be transmitted. Provide the parallel interface between transmit shift register and internal bus. If the check bit is turned on when transmitting data, it is invalid to write to the most significant bit, and it will be replaced by the check bit and transmitted again.
31:9	Reserved		

22 Internal Integrated Circuit Interface (I2C)

The C6T6 of the APM32F030x4x6x8 A version chip has only I2C1, while the B version has two I2C, other configurations are consistent.

22.1 Full Name and Abbreviation Description of Terms

Table 69 Full Name and Abbreviation Description of Terms

Full name in English	English abbreviation
Serial Data	SDA
Serial Clock	SCL
System Management Bus	SMBus
Clock	CLK
Serial Clock High	SCLH
Serial Clock Low	SCLL
Address Resolution Protocol	ARP
Negative Acknowledgement	NACK
Packet Error Checking	PEC

22.2 Introduction

I2C is a short-distance bus communication protocol. In physical implementation, I2C bus is composed of two signal lines (SDA and SCL) and a ground wire. These two signal lines can be used for bidirectional transmission.

- Two signal lines, SCL clock line and SDA data line. SCL provides timing for SDA, and SDA transmits/receives data in series.
- Both SCL and SDA signal lines are bidirectional.
- The ground is common when the two systems use I2C bus for communication.

22.3 Main Characteristics

（1） Can select master or slave mode

（2） Multi-master function

（3） 7-bit and 10-bit addressing mode

（4） Response to broadcast

（5） Multiple 7-bit slave address

（6） Three communication speeds

- Standard mode
- Fast mode
- Fast mode plus

（7） Programmable clock extension

（8） Programmable start time and hold time

（9） Support DMA function

（10） Programmable noise filter

- EC error check

（11） SMBus specific function

- Hardware PEC
- Address resolution protocol
- HOST notification protocol
- SMBus alarm
- SMBus timeout management

（12） Can select an independent clock source

22.4 Structure Block Diagram

Figure 90 I2C1 Functional Structure Diagram

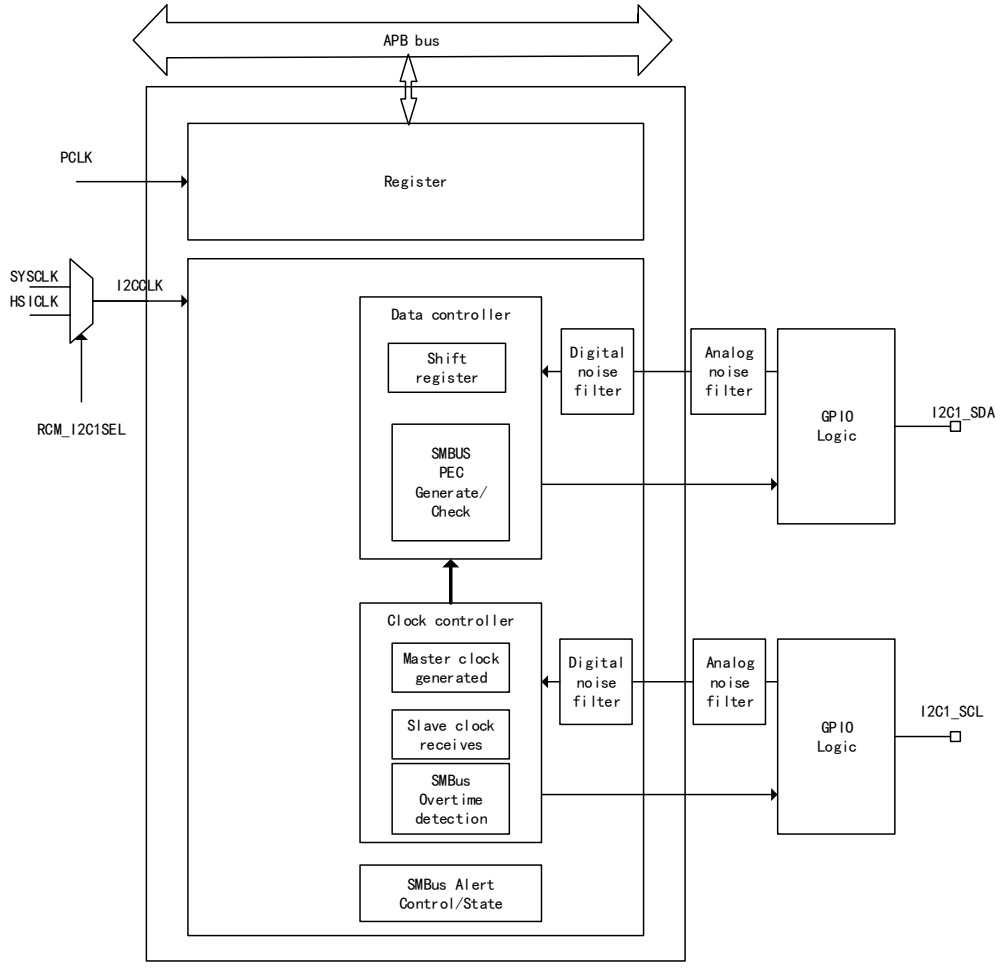
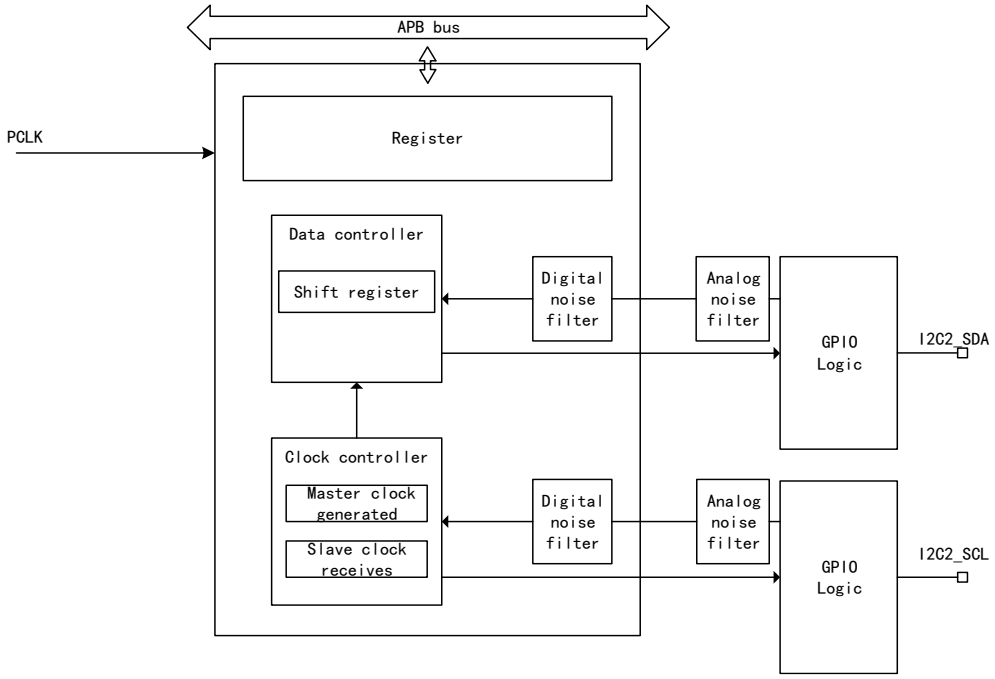


Figure 91 I2C2 Functional Structure Diagram



22.5 Functional Description

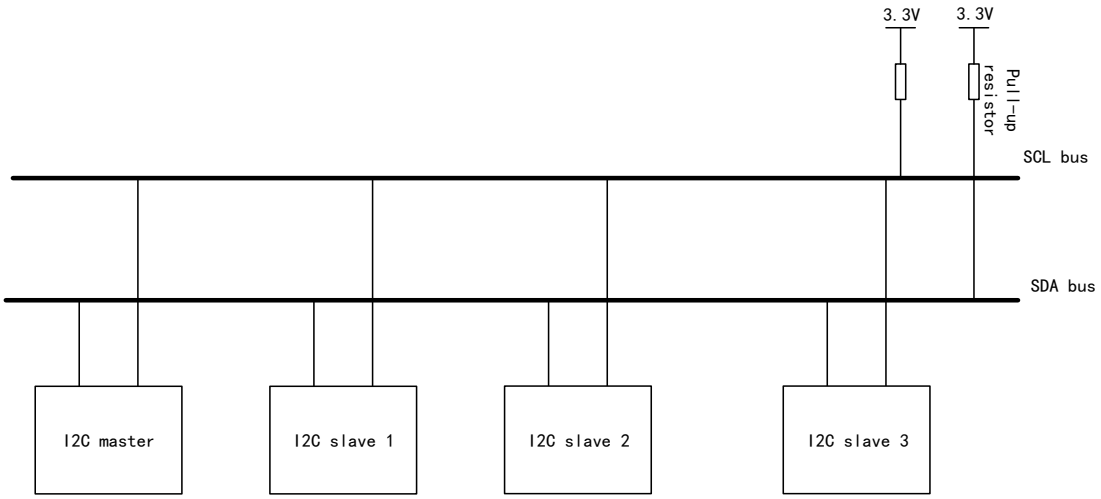
Table 70 Description of I2C bus terms

proper terms	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Master	The device that initializes the data transmission, generates the clock signal, and ends the data transmission
Slave	Devices addressed by the master
Multimaster	Multiple masters that control the bus at the same time without destroying information
Synchronization	The process of synchronizing clock signals between two or more devices
Arbitration	If more than one master attempts to control the bus at the same time, only one host can control it, and the controlled host information is not destroyed

22.5.1 I2C Physical Layer

Common connections between I2C communication devices are as follows:

Figure 92 Commonly Used I2C Communication Connection Diagram



Characteristics of physical layer

（1） Bus supporting multiple devices (signal line shared by multiple devices), which, in I2C communication bus, can connect multiple communication masters and communication slaves.

（2） An I2C bus only uses two bus lines, namely, a bidirectional serial data line (SDA) and a serial clock line (SCL). The data line is used for data transmission, and the clock line is used for synchronous receiving and transmission of data.

（3） Each device connected to the bus has an independent address (seven or ten bits), and the master addresses and accesses the slave device according to the address of the device.

（4） The bus needs to connect the pull-up resistor to the power supply. When I2C bus is idle, the output is in high-impedance state. When all devices are idle, the output is in high-impedance state, and the pull-up resistor pulls the bus to high level.

（5） Three communication modes: Standard mode (up to 100KHz), fast mode (up to 400KHz), and fast mode plus (up to 1MHz).

（6） When multiple masters use the bus at the same time, to prevent the data conflict, the bus arbitration mode is adopted to determine which device occupies the bus.

（7） Can program setup and hold time, and program the high-level time and low-level time of SCL in I2C.

22.5.2 I2C Protocol Layer

Characteristics of protocol layer

（1） Data is transmitted in the form of frame, and each frame is composed of 1 byte (8 bits).

（2） In the rising edge phase of SCL, SDA needs to keep stable and SDA changes during the period when SCL is low.

（3） In addition to data frame, I2C bus also has start signal, stop signal and acknowledge signal.

- Start bit: During the stable high level period of SCL, a falling edge of SDA starts transmission.
- Stop bit: During the stable high level period of SCL, a rising edge of SDA stops transmission.
- Acknowledge bit: Used to indicate successful transmission of one byte. After the bus transmitter (regardless of the master or slave) transmits 8-bit data, SDA will release (from output to input). During the ninth clock pulse, the receiver will pull down SDA to respond to the received data.

I2C communication reading and writing process

Figure 93 Master Writes Data to Slave

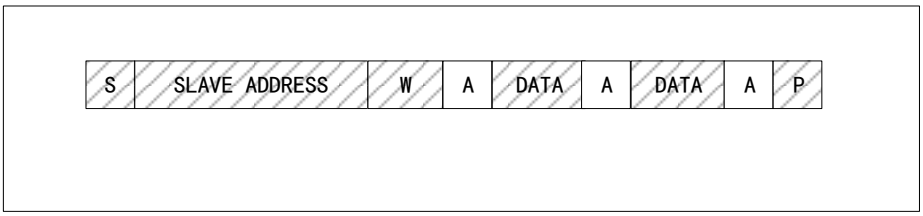
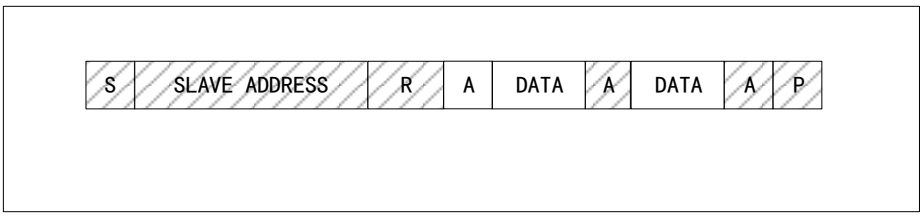


Figure 94 Master Reads Data from Slave



Note:

（1）  : This data is transferred from master to slave

（2）S: Start signal

（3）SLAVE ADDRESS: Slave address

（4）  : This data is transferred from slave to master

（5）R/W: Selection bit of transmission direction

（6）1 means reading

（7）0 means writing

（8）P: Stop signal

After the start signal is generated, all slaves will wait for the slave address signal transmitted by the master. In I2C bus, the address of each device is unique. When the address signal matches the device address, the slave will be selected, and the unselected slave will ignore the future data signal.

When the transmission direction is writing data

After broadcasting the address and receiving the acknowledge signal, the master will transmit data to the slave, the data length is one byte, and every time the master transmits one byte of data, it needs to wait for the answer signal transmitted by the slave. After all the bytes have been transmitted, the master will transmit a stop signal (STOP) to the slave, indicating that the transmission is completed.

When the transmission direction is reading data

After broadcasting the address and receiving the acknowledge signal, the slave will transmit the data to the master. The size of the data package is 8 bits. Every time the master sends one byte of data, it needs to wait for the acknowledge signal of the slave. When the master wants to stop receiving data, it needs to return a non-answer signal to the slave, then the slave will stop transmitting the data automatically.

22.5.3 Introduction to I2C Clock

22.5.3.1 I2C clock source

I2C is driven by an independent clock source, and it can make I2C1 operate independent of PCLK frequency.

I2C clock source can select HSICLK or SYSCLK.

22.5.3.2 Requirements for I2C clock

（1） $t_{I2C\_CLK} < (t_{low}-t_{filters})/4$ and $t_{I2C\_CLK} < t_{HIGH}$

（2） t_{low}: SCL low-level time

（3） t_{HIGH}: SCL high-level time

（4） $t_{filters}$: Total lag caused by analog filter and digital filter when I2C is started

I2C clock configuration

Before peripherals are started, it is required to configure SCLH and SCLL bits in I2C_TIMING register to configure the I2C clock.

It can realize clock synchronization mechanism and support multiple master environments and slave clock extension.

$t_{SCL}=t_{SYNC1}+t_{SYNC2}+\{（（SCLH+1）+（SCLL+1））*（TIMINGPSC+1）* t_{I2C\_CLK}\}$

t_{SYNC1} depends on:

- SCL descending slope
- Input delay of analog filter
- Input delay of digital filter
- Delay caused by synchronous I2C_CLK clock of SCL

t_{SYNC2} depends on:

- SCL rising slope:
- Input delay of analog filter
- Input delay of digital filter
- Delay caused by synchronous I2C_CLK clock of SCL

To make I2C compatible with SMBus mode, the requirements for clock timing are shown in the table below:

Table 71 Clock Timing Requirement

Symbol	Parameter	Standard mode		Fast mode		Fast mode plus		SMBus		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	-	100	-	400	-	1000	-	100	KHz
$t_{HD:STA}$	START signal hold time	4	-	0.6	-	0.26	-	4.0	-	μs
$t_{SU:STA}$	START signal setup time	5	-	0.6	-	0.26	-	4.7	-	μs
$t_{SU:STO}$	STOP signal setup time	4	-	0.6	-	0.26	-	4.7	-	μs
t_{BUF}	Idle time of bus between STOP and START signals	5	-	1.3	-	0.50	-	4.0	-	μs
t_{LOW}	SCL clock low-level time	8	-	1.3	-	0.50	-	4.7	-	μs
t_{HIGH}	SCL clock high-level time	4	-	0.6	-	0.26	-	4.0	50	μs
t_r	Rising edge time of SDA and SCL signals	-	1000	-	300	-	120	-	1000	ns
t_f	Falling edge time of SDA and SCL signals	-	300	-	300	-	120	-	300	ns

22.5.3.3 I2C_TIMING register configuration

Table 72 I2C_TIMING Register Configuration

f_{I2C_CLK} =72MHz				
Parameter	Standard mode		Fast mode	Fast mode plus
	10 KHz	100 KHz	400 KHz	1 MHz
TIMINGPSC	0xF	0x8	8	8
SCLL	0xD8	0x27	0x9	0x3
t_{SCLL}	217x222ns=48.174μs	40x125ns=5μs	10x125ns = 1250 ns	4x125 ns =500 ns
SCLH	0xD8	0xF	0x3	0x1
t_{SCLH}	217x222ns=48.174μs	16x125ns=2μs	4x125 ns = 500 ns	2x125 ns = 250 ns
t_{SCL}	100μs	10μs	2500ns	875ns
DATAHT	0x5	0xC	0x3	0
t_{DATAHT}	5x222ns=1.11μs	12x125ns=1.5μs	3x125 ns = 375 ns	0ns
DATAT	0x5	0x4	0x3	0x1

f_{I2C_CLK} =72MHz				
t_{DATAT}	6x222ns=1.332μs	5x125ns=625ns	4x125 ns = 500 ns	2x125 ns = 250 ns

Note:

t_{I2C_CLK} = 1/ f_{I2C_CLK}

$t_{TIMINGPSC}$ =（TIMINGPSC+1）x t_{I2C_CLK}

t_{DATAT} =（DATAT+1）x $t_{TIMINGPSC}$

t_{DATAHT} =（DATAHT）x $t_{TIMINGPSC}$

t_{SCLH} =（SCLH+1）x $t_{TIMINGPSC}$

t_{SCLL} =（SCLL+1）x $t_{TIMINGPSC}$

22.5.4 I2C Function Configuration Mode

The interface can be configured to the following modes:

- Slave transmitting
- Slave receiving
- Master transmitting
- Master receiving

In the initial state of I2C interface, the working mode is slave mode. After I2C interface sends the start signal, it will automatically switch from slave mode to master mode.

22.5.4.1 Slave mode

Transmitt in slave mode

After the master sends the start signal and address, the addressing is successful, the ADDRMFLG bit is cleared, and the transmitter will transmit the data to be transmitted from I2C_TXDATA register to SDA line by internal shift register.

Every time the slave sends a byte, it will wait for the master's acknowledge signal (ACK) and repeat this process until the master wants to stop receiving data and returns a non-acknowledge signal (NACK) to the slave. At this time, the slave will stop data transmission.

Receive in slave mode

After receiving the address of the master, ADDRMFLG bit will be cleared, and the data received by the slave from the SDA line through the internal shift register are stored in I2C_RXDATA register.

After the slave receives a byte, it will send an acknowledge signal (ACK) to the master and when the master sends a stop signal, the transmission is over.

Extension of slave clock

In default mode, I2C slave will pull down SCL clock in the following situations:

- The received address matches the enabled slave address, and SCL clock is pulled down and will be released when ADDRMFLG flag is

cleared by software. ADDRMFLG flag bit can be cleared by setting ADDRMCLR bit to 1.

- When transmitting, if the previous data have been transmitted and no new data are written to I2C_TXDATA register, or ADDRMFLG flag is cleared, and no byte is written to I2C_TXDATA register, the SCL clock will be pulled down and when data are written to I2C_TXDATA register, the SCL clock will be released.
- When receiving, if the content of I2C_RXDATA register is not read and new data are received, the SCL clock will be pulled down and when I2C_RXDATA register is read, the SCL clock will be released.

22.5.4.2 Master mode

Master transmitting

I2C interface sends the start signal and sends the address to the SDA line through the internal shift register. The transmission direction is write, waiting for the slave to respond. After the slave responds, the master will send bytes from I2C_TXDATA register to SDA line through the internal shift register and wait for the acknowledge signal (ACK) transmitted by slave, and so forth. When I2C_TXDATA register writes the last byte, the stop bit is set to generate a stop signal.

Master receiving

The I2C interface sends the start signal and sends the address to the SDA line through the internal shift register. The transmission direction is read. After the slave responds, the master enters the receiving mode, receives the data on the SDA line through the internal shift register and sends them to I2C_RXDATA register. Every time the master receives a data, it will return an acknowledge signal (ACK). This process will be repeated and when the master needs to stop reading data, it will send a non-acknowledge signal (NACK) to stop reading data.

22.5.4.3 SMBus specific function

The system management bus (SMBus) is a two-wire interface, which is based on I2C bus principle.

The system management bus specification refers to three types of devices

Slave: Device of receiving or corresponding command.

Master: Device that issues commands, generates clocks and terminates transmission.

HOST: A special master, which provides interfaces to system CPU. The HOST must have dual functions of master and slave, and support SMBus HOST notification protocol, and one system has only one HOST.

Bus protocol

There are 11 possible command protocols for any given device, and one device can communicate with any or all of 11 protocols.

Address resolution protocol (ARP)

SMBus slave address conflict can be solved by calibrating a new unique address for the slave device. In order to assign addresses, a mechanism is needed to distinguish each device, and each device has a unique device identifier. The 128-bit identifier is implemented by software.

This device supports address resolution protocol (ARP). Set DEADDREN bit in I2C_CTRL1 register to 1, and the default address of SMBus device (0b1100001) will be enabled. ARP command is implemented by user software.

The arbitration supported by ARP is also completed in slave mode.

Command receiving and data acknowledgment control

SMBus receiver will return NACK to each command and data received. Start the ACK control in slave mode, and set SBCEN bit of I2C_CTRL1 register to 1 to start the slave byte control mode.

HOST notification protocol

Set HADDREN bit of I2C_CTRL1 register to make this peripheral support HOST notification protocol. In such case, HOST will acknowledge SMBus host slave (0b0001000).

Use this protocol, this device is used as the master, and HOST is used as the slave.

SMBus alarm

This peripheral can be supported by SMBus reminder signal. When a device that is used only as the slave wants to initiate communication, it can notify HOST through SMBALERT pin. HOST will handle the interrupt and then access all SMBA devices through the reminder response address (0b0001100). Only the device with the SMBA pin pulled down will respond to the reminder response address.

SMBus timeout management

Table 73 SMBus Timeout Specification

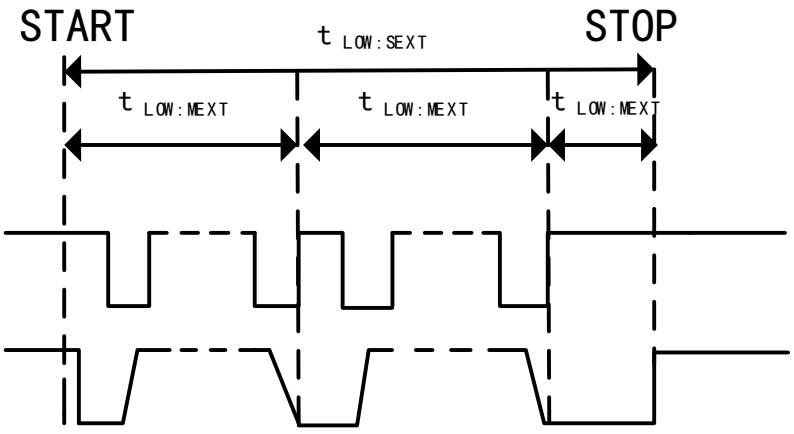
Symbol	Parameter	Range		Unit
		Min	Max	
$t_{TIMEOUT}$	Low timeout of detection clock	25	35	ms
$t_{LOW:SEXT}$	Low extension time of cumulative clock of slave	-	25	ms
$t_{LOW:MEXT}$	Low extension time of cumulative clock of master	-	10	ms

$t_{LOW:SEXT}$ is an extensible clock cycle accumulation given by a slave device from START to STOP. When a slave device or a master device occupies the clock, the total low clock time is greater than $t_{LOW:SEXT}$. Therefore, the test condition of this parameter is that the slave is the only communication target of a full-speed master.

$t_{LOW:MEXT}$ is the clock cycle accumulation allowed by a master device to send a byte in the way of from START to ACK, from ACK to ACK, from ACK to STOP. When another slave device or master occupies the clock, the total time occupies by the clock may also be greater than $t_{LOW:MEXT}$. Therefore, the measurement

condition of this parameter is that only one full-speed slave is the only communication target.

Figure 95 $t_{LOW:SEXT}$ and $t_{LOW:MEXT}$ Time



22.5.4.4 Error flag bit

I2C communication has the following error flag bits that may cause communication failure.

Bus error flag bit (BERRFLG)

When a START or STOP condition is detected outside 9 times of SCL clock pulse signal, a bus error will occur. When SCL is high and a rising or falling edge occurs on SDA, it will be detected as START or STOP signal.

Only when I2C is communicating and transmitting data, can bus error occur (after data have been transmitted as the master or the address has matched as the slave). This error will not occur in slave mode address matching phase.

When a bus error is detected, BERRFLG flag bit of I2C_STS register will be set to 1 by hardware; if ERRIEN bit of I2C_CTRL1 register is set to 1, an error interrupt will be generated.

Arbitration loss flag bit (ALFLG)

When a high level is transmitted on the SDA line, but the rising edge of SCL samples a low level from SDA, it will be detected as an arbitration loss error.

- In master mode, arbitration loss is detected in address phase, data phase and data validation phase. In such case, SDA and SCL lines will be released, the START control bit will be cleared by hardware, and the master mode is automatically switched to slave mode.
- In slave mode, arbitration loss is detected in data phase and data validation phase. In this case, transmission is terminated and SCL and SDA lines are released.

When an arbitration loss error is detected, ALFLG flag bit of I2C_STS register will be set to 1 by hardware; if ERRIEN bit of I2C_CTRL1 register is set to 1, an error interrupt will be generated.

Overrun/Underrun error flag bit (OVRURFLG)

When clock extension is disabled (CLKSTRETCHD=1), underrun or overrun error

will be detected under the following conditions in slave mode

- When receiving, the RXDATA register has not been read, but the newly transmitted byte has been received.
- When transmitting, the first data byte should be transmitted, but STOPFLG=1. If TXBEFLG=0, the value of I2C_TXDATA register is transmitted; if it is not 0, then 0xFF is transmitted.
- When transmitting, if a new byte should be written to I2C_TXDATA register, but it is not written, 0xFF will be transmitted.

When an overrun/underrun error is detected, OVRURFLG flag of I2C_STS register will be set to 1 by hardware; if ERRIEN bit of I2C_CTRL1 register is set to 1, an interrupt will be generated.

Packet error check error flag bit (PECEFLG)

This error condition is only for SMBus function part. After receiving PEC byte not matching the content of I2C_PEC register, PEC error will be detected. After the error PEC is received, a NACK will be returned automatically. When PEC error is detected, PECEFLG flag of I2C_STS register will be set to 1 by hardware; if ERRIEN bit of I2C_CTRL1 register is set to 1, an interrupt will be generated.

Timeout error flag bit (TTEFLG)

This error condition is only for SMBus function part.

Timeout error will occur under the following conditions

（1） SMBus timeout is detected

- IDLECLKTO=0 and the hold time of low SCL reaches the time defined by TIMEOUTA[11:0] bit field.
- IDLECLKTO=1 and the high-level time of SDA and SCL exceeds the time defined by TIMEOUTA[11:0] bit field.

（2） SMBus idle timeout is detected

- The accumulative time of low extension of master clock reaches the time ($t_{LOW:MEXT}$) defined by TIMEOUTB[11:0] bit field.
- The accumulative time of low extension of slave clock reaches the time ($t_{LOW:SEXT}$) defined by TIMEOUTB[11:0] bit field.

When a TIMEOUT error is detected, TTEFLG flag of I2C_STS register will be set to 1 by hardware; if ERRIEN bit of I2C_CTRL1 register is set to 1, an interrupt will be generated.

22.5.4.5 DMA request

DMA transmission can be enabled by setting DMATXEN bit of I2C_CTRL1 register. The data is put into the SRAM area set by DMA peripheral in advance and transmitted to I2C_TXDATA register (not needing to consider the state of TXINTFLG bit).

Only use DMA to transmit bytes:

- Master mode: Initialization, slave address, direction, byte number and start bit are set by software (when the slave address has been transmitted, DMA cannot be used for transmission). When all data are transmitted by DMA, DMA must be initialized before START bit is set to 1.
- Slave mode: DMA must be initialized before the address matching event.

22.5.5 I2C Interrupt

Table 74 Interrupt Request List

Interrupt event	Event flag bit	Method of clearing the event flag bit	Interrupt enable control bit
Received character is not empty	RXBNEFLG	Read I2C_RXDATA register	RXIEN
Transmit interrupt state	TXINTFLG	Write I2C_TXDATA register	TXIEN
Stop signal detection flag	STOPFLG	Write STOPCLR=1	STOPIEN
Transmission completion reload	TXCRFLG	Write I2C_CTRL2 and NUMBYT[7:0] is not 0	TXCIEN
Transmission completed	TXCFLG	Write START=1 or STOP=1	
Address match	ADDRMFLG	Write ADDRMCLR=1	SADDRMIEN
Receive NACK flag bit	NACKFLG	Write NACKCLR=1	NACKRXIEN
Bus error	BERRFLG	Write BERRCLR=1	ERRIEN
Arbitration loss	ALFLG	Write ALCLR=1	
Overrun/Underrun error	OVRURFLG	Write OVRURCLR=1	
PEC error	PECEFLG	Write PECECLR=1	
Clock timeout	TTEFLG	Write TTECLR=1	
SMBus reminder	SMBALTFLG	Write SMBALTCLR=1	

To enable I2C interrupt, it is required to:

- Configure and start I2C channel in NVIC
- Configure I2C interrupt enable bit

22.6 Register Address Mapping

Table 75 I2C Register Address Mapping

Register name	Description	Offset address
I2C_CTRL1	Control register 1	0x00
I2C_CTRL2	Control register 2	0x04
I2C_ADDR1	Master address register 1	0x08
I2C_ADDR2	Master address register 2	0x0C
I2C_TIMING	Timing register	0x10
I2C_TIMEOUT	Timeout register	0x14
I2C_STS	State register	0x18
I2C_INTFCLR	Interrupt flag clear register	0x1C
I2C_PEC	PEC register	0x20
I2C_RXDATA	Receive data register	0x24

Register name	Description	Offset address
I2C_TXDATA	Transmit data register	0x28

22.7 Register Functional Description

22.7.1 Control register 1 (I2C_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	I2CEN	R/W	I2C Enable 0: Disable 1: Enable
1	TXIEN	R/W	Transmit Interrupt Enable 0: Disable 1: Enable
2	RXIEN	R/W	RX Interrupt Enable 0: Disable 1: Enable
3	SADDRMIEN	R/W	Slave Address Match Interrupt Enable 0: Disable 1: Enable
4	NACKRXIEN	R/W	NACK Received Interrupt Enable 0: Disable 1: Enable
5	STOPIEN	R/W	STOP Detection Interrupt Enable 0: Disable 1: Enable
6	TXCIEN	R/W	Transmit Complete Interrupt Enable 0: Disable 1: Enable
7	ERRIEN	R/W	Error Interrupt Enable 0: Disable 1: When the position 1 of any of the following state register is enabled, the interrupt will be generated: SMBALTFLG, TTEFLG, PECEFLG, OVRURFLG, ALFLG, and STS1_BERRFLG
11:8	DNFCFG	R/W	Digital Noise Filter Configure The digital noise filters of SDA and SCL are configured by this bit field. The length of digital filter is DNFCFG[3:0]*t_{I2C_CLK}. 0000: Disable 0001: Enabled; one t_{I2C_CLK} …… 1111:Enabled; 15 t_{I2C_CLK} If the analog filter is enabled at the same time, the digital filter will be added to the analog filter; This bit can be set only when I2CEN is not set.
12	ANFD	R/W	Analog Noise Filter Disable 0: Enable 1: Disable This bit can be set only when I2CEN is not set.
13	Reserved		
14	DMATXEN	R/W	DMA Transmit Enable 0: Disable 1: Enable
15	DMARXEN	R/W	DMA Receive Enable 0: Disable 1: Enable

Field	Name	R/W	Description
16	SBCEN	R/W	Slave Byte Control Enable 0: Disable 1: Enable
17	CLKSTRETCHD	R/W	Slave Mode Clock Stretching Disable 0: Enable 1: Disable This bit can be set only when I2CEN is not set, and it is applicable only to the slave mode.
18	Reserved		
19	RBEN	R/W	Responds Broadcast Enable The address of response to broadcast is 0x00. 0: Disable 1: Enable
20	HADDREN	R/W	SMBus Host Address Enable The HOST address is 0x10/0x11. 0: Disable 1: Enable If SMBus mode is not supported, this bit will be reserved and be forced to 0.
21	DEADDREN	R/W	SMBus Device Default Address Enable The default address is 0xC2/0xC3. 0: Disable 1: Enable If SMBus mode is not supported, this bit will be reserved and be forced to 0.
22	ALTEN	R/W	SMBus Alert Function Enable Device mode (HADDREN=0): 0: Release SMBALERT pin and disable the notification response address header after NACK. 1: Pull down SMBALERT pin and enable the notification response address header after ACK. HOST mode (HADDREN=1): 0: Not supported 1: Supported If ALTEN=0, SMBALERT pin can be used as a GPIO; If SMBus mode is not supported, this bit will be reserved and be forced to 0.
23	PECEN	R/W	PEC Enable 0: Disable 1: Enable If SMBus mode is not supported, this bit will be reserved and be forced to 0.
31:24	Reserved		

22.7.2 Control register 2 (I2C_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	SADDR[0]	R/W	Slave Address Setup When the address mode is 7 bits, the bit is invalid; when the address mode is 10 bits, this bit is The bit 0 of the address.
7:1	SADDR[7:1]	R/W	Slave Address Setup The bit [7:1] of slave address.
9:8	SADDR[9:8]	R/W	Slave Address Setup

Field	Name	R/W	Description
			When the address mode is 7 bits, the bit is invalid; when the address mode is 10 bits, this bit is the 9:8 bit of the address.
10	TXDIR	R/W	Master Mode Transfer Direction Setup 0: Write transmission 1: Read transmission
11	SADDRLEN	R/W	Slave Address Length Configure 0: 7-bit addressing mode 1: 10-bit addressing mode
12	ADDR10	R/W	Master Transmit 10-Bit Address Header Configure 0: Transmit 10-bit slave address read sequence: start bit + 2-byte 10-bit write direction address + restart + the first 7 bits of 10-bit read direction address. 1: Transmit the first 7 bits of 10-bit slave address read sequence + read direction.
13	START	R/W	Start Bit Transfer This bit can be set to 1 and cleared by software; it can be cleared by hardware after the start bit and address sequence are transmitted, arbitration loss occurs, timeout error occurs or I2CEN bit is not set, or be cleared by setting ADDRMCLR bit of I2C_INTFCLR register. In master mode: 0: Not send 1: Transmit repeatedly In slave mode: 0: Not send 1: Transmit when the bus is idle It is meaningless to write 0 to this bit; Setting RELOAD bit and this bit does not work.
14	STOP	R/W	Stop Bit Transfer This bit can be set to 1 and cleared by software; it can be cleared by hardware when transmitting the stop bit or when I2CEN bit is not set. In master mode: 0: Not transfer 1: Transfer It is meaningless to write 0 to this bit.
15	NACKEN	R/W	Transmit NACK Enable This bit can be set to 1 and cleared by software; it can be cleared by hardware after the stop bit and NACK are transmitted, the address match event is received or when I2CEN bit is not set. 0: Transmit ACK 1: Transmit NACK It is meaningless to write 0 to this bit, and it is applicable only to the slave ode. In master receiving mode, it will be automatically transmitted after the last byte is transmitted and between transmitting the stop bit or RESTART bit. In slave receiving mode, NACK will be transmitted automatically when overrun occurs. In this case, NACKEN bit does not work; After PEC check of hardware is enabled, the confirmation value of PEC still does not depend on the value of NACK bit.
23:16	NUMBYT	R/W	Number of Bytes Setup This bit determines the number of bytes to be transmitted. This bit is meaningless when it is in slave mode and SBCEN=0. This bit can be set only when START bit is not set.

Field	Name	R/W	Description
24	RELOADEN	R/W	NUMBYT Reload Mode Enable It can be set to 1 and cleared by software. 0: Transmission is over after transmission of NUMBYT bytes 1: Reload NUMBYT after transmission of NUMBYT bytes. After transmission of NUMBYT bytes, TXCFLG flag bit will be set and SCL will be pulled down.
25	ENDCFG	R/W	End Mode Configure It can be set to 1 and cleared by software. 0: Software end mode: after transmission of NUMBYT data, TXCFLG flag bit will be set, and SCL will be pulled down. 1: Automatic end mode: after transmission of NUMBYT data, a stop bit will be transmitted automatically. This bit does not work when it is in slave mode or RELOADEN bit is set.
26	PEC	R/W	Transfer Packet Error Checking Byte Enable This bit can be set to 1 and cleared by software; it can be cleared by hardware after PEC transmission is completed, the stop bit is received, the address match event is received or when I2CEN bit is not set. 0: Disable 1: Enable It is meaningless to write 0 to this bit. Set RELOADEN bit or clear SBCEN bit in slave mode and this bit will not work; If SMBus mode is not supported, this bit will be reserved and be forced to 0.
31:27	Reserved		

22.7.3 Master address register 1 (I2C_ADDR1)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ADDR1[0]	R/W	Master Address Setup When the address mode is 7 bits, the bit is invalid; when the address mode is 10 bits, this bit is the 0 bit of the address.
7:1	ADDR1[7:1]	R/W	Master Address Setup The bit[7:1] of master address
9:8	ADDR1[9:8]	R/W	Master Address Setup When the address mode is 7 bits, the bit is invalid; when the address mode is 10 bits, this bit is the bit [9:8] of the address.
10	ADDR1LEN	R/W	Master Address Length Configure 0: 7-bit addressing mode 1: 10-bit addressing mode
14:11	Reserved		
15	ADDR1EN	R/W	Master Address 1 Enable 0: Disable. Transfer NACK after the slave address ADDR is received 1: Enable. Transfer ACK after the slave address ADDR is received
31:16	Reserved		

22.7.4 Master address register 2 (I2C_ADDR2)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	Reserved		
7:1	ADDR2[7:1]	R/W	Master Address Setup Master address bit [7:1]
10:8	ADDR2MSK	R/W	Masks Master Address 2 Select 000: No mask 001: Mask ADDR2[1], compared with ADDR2[7:2]. 010: Mask ADDR2[2:1], compared with ADDR2[7:3]. 011: Mask ADDR2[3:1], compared with ADDR2[7:4]. 100: Mask ADDR2[4:1], compared with ADDR2[7:5]. 101: Mask ADDR2[5:1], compared with ADDR2[7:6]. 110: Mask ADDR2[6:1], compared with ADDR2[7]. 111: Mask ADDR2[7:1], without comparison; all 7-bit addresses received will send ACK. This bit can be set only when ADDR2EN bit is not set; if ADDR2MSK is not 0, and the reserved I2C address does not response, matching is meaningless.
14:11	Reserved		
15	ADDR2EN	R/W	Master Address 2 Enable 0: Disable. Send NACK after the slave address ADDR2 is received. 1: Enable. Send ACK after receiving the slave address ADDR2.
31:16	Reserved		

22.7.5 Timing register (I2C_TIMING)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	SCLL	R/W	SCL Low Level Time Setup t_{SCLL} =(SCLL+1) x $t_{TIMINGPSC}$ SCLL determines t_{BUF} and $t_{SU:STA}$ timing.
15:8	SCLH	R/W	SCL High Level Time Setup t_{SCLH} =(SCLH+1) x $t_{TIMINGPSC}$ SCLH determines $t_{SU:STO}$ and $t_{HD:STA}$ timing.
19:16	DATAHT	R/W	Data Hold Time Setup This bit field determines the delay t_{DATAHT} between SCL falling edge and SDA edge in transmit mode. t_{DATAHT}=DATAHT x $t_{TIMINGPSC}$ DATAHT determines $t_{HD:DAT}$ timing.
23:20	DATAT	R/W	Data Time Setup This bit field determines the delay t_{DATAT} between SDA edge and SCL rising edge in transmit mode. t_{DATAT}=(DATAT+1) x $t_{TIMINGPSC}$ t_{DATAT} determines $t_{SU:DAT}$ timing.

Field	Name	R/W	Description
27:24	Reserved		
31:28	TIMINGPSC	R/W	Timing Prescaler Setup This bit field divides the frequency of I2C_CLK, and provides clock cycle $t_{TIMINGPSC}$ for data setup, hold time counter and SCL high and low-level counter. $t_{TIMINGPSC}$=(TIMINGPSC+1) x t_{I2C_CLK}。

Note: This register can be set only when I2CEN bit is not set.

22.7.6 Timeout register (I2C_TIMEOUT)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
11:0	TIMEOUTA	R/W	Bus Timeout A Setup When IDLECLKTO=0, and SCL timeout is low: $t_{TIMEOUT}$=(TIMEOUTA+1) x 2048 x t_{I2C_CLK} When IDLECLKTO=1, and the bus is idle: t_{IDLE}=(TIMEOUTA+1) x 4 x t_{I2C_CLK} This bit can be set only when CLKTOEN bit is not set.
12	IDLECLKTO	R/W	Idle Clock Timeout Detection Configure 0: SCL low-level timeout is detected 1: SCL and SDA high-level timeout is detected (the bus is idle) This bit can be set only when CLKTOEN bit is not set.
14:13	Reserved		
15	CLKTOEN	R/W	Clock Timeout Enable 0: Disable 1: Enable. A timeout error is detected when the hold time of low SCL is more than $t_{TIMEOUT}$ or the hold time of high SCL is more than t_{IDLE}.
27:16	TIMEOUTB	R/W	Bus Timeout B Setup The accumulated master clock low extension time to be detected in master mode ($t_{LOW:MEXT}$). The accumulated slave clock low extension time to be detected in slave mode ($t_{LOW:SEXT}$). $t_{TLOW:EXT}$=(TIMEOUTB+1) x 2048 x t_{I2C_CLK} This bit field can be set only when EXCLKTOEN bit is not set.
30:28	Reserved		
31	EXCLKTOEN	R/W	Extended Clock Timeout Enable 0: Disable 1: Enable. A timeout error is detected when the hold time of low SCL reaches $t_{TLOW:EXT}$.

22.7.7 State register (I2C_STS)

Offset address: 0x18

Reset value: 0x0000 0001

Field	Name	R/W	Description
0	TXBEFLG	R/S	Transmit Data Buffer Empty Flag 0: The transmit buffer is not empty 1: The transmit buffer is empty This bit is set to 1 by hardware when the content of I2C_TXDATA register is empty; this bit is cleared when the data to be transmitted are written to I2C_TXDATA register.

Field	Name	R/W	Description
			This bit can be set to 1 by software to clear I2C_TXDATA register; when I2CEN=0, this bit is cleared by hardware.
1	TXINTFLG	R/S	Transmit Interrupt State Flag 0: Not transmit 1: Send This bit is set to 1 by hardware when I2C_TXDATA register is empty; then write the data to be transmitted to I2C_TXDATA register. This bit can be cleared by writing the data to be transmitted to I2C_TXDATA register. This bit can be set to 1 by software when CLKSTRETCHD=1, so as to generate TXINTFLG flag bit; it can be cleared by hardware when I2CEN=0.
2	RXBNEFLG	R	Receive Data Buffer Not Empty Flag 0: The receive buffer is empty 1: The receive buffer is not empty This bit can be set to 1 by hardware when there are data in RXDATA register; this bit can be cleared by reading I2C_RXDATA; and be cleared by hardware when I2CEN=0.
3	ADDRMFLG	R	Slave Address Match Flag 0: The slave address does not match 1: The slave address matches When the received slave address matches any valid slave address, this bit is set to 1 by hardware. This bit can be cleared by software by setting ADDRMCLR bit to 1; or be cleared by hardware when I2CEN=0.
4	NACKFLG	R	Receive Not Acknowledge Flag 0: NACK flag is not received 1: NACK flag is received This bit can be set to 1 by hardware when one byte is transmitted and NACK is received. It can be cleared by software by setting NACKCLR bit to 1; or be cleared by hardware when I2CEN=0.
5	STOPFLG	R	Stop Bit Detection Flag 0: No stop bit is detected 1: The stop bit is detected This bit can be set to 1 by hardware when the peripheral participates in transmission and the stop bit is detected on the bus. This bit can be cleared by software if the peripheral sends the stop bit as the master or the peripheral is addressed correctly as the slave before this transmission, and STOPCLR=1; or be cleared by hardware when I2CEN=0.
6	TXCFLG	R	Transmit Data Complete Flag 0: Transmit data is not completed 1: Transmit data is completed This bit can be set to 1 by hardware when RELOADEN=0, ENDCFG=0 and NUMBYT data have been transmitted; be cleared when START=1 or STOP=1; or be cleared by hardware when I2CEN=0.
7	TXCRFLG	R	Transfer Complete Reload Flag 0: Transmission is completed 1: Transmission is completed to reload This bit can be set to 1 by hardware when RELOADEN=1 and NUMBYT data have been transmitted; it can be cleared by software by writing a non-zero value to NUMBYT; or be cleared by hardware when I2CEN=0. This bit works only in master mode, or in slave mode when SBCEN=1.
8	BERRFLG	R	Bus Error Flag 0: No bus error 1: Bus error occurred

Field	Name	R/W	Description
			This bit can be set to 1 by hardware when wrong start bit or stop bit is detected; be cleared by software by setting BERRCLR bit; or be cleared by hardware when I2CEN=0.
9	ALFLG	R	Arbitration Lost Flag 0: No arbitration loss 1: Arbitration loss occurred This bit can be set to 1 by hardware when bus arbitration loss occurs; be cleared by software by setting ALCLR bit; or be cleared by hardware when I2CEN=0.
10	OVRURFLG	R	Overrun/Underrun Flag 0: No overrun/underrun 1: Overrun/Underrun occurs This bit can be set to 1 by hardware if overrun/underrun error occurs in slave mode when CLKSTRETCHD=1; be cleared by software by setting OVRURCLR bit; and be cleared by hardware when I2CEN=0.
11	PECEFLG	R	PEC Error in Reception Flag 0: No PEC error 1: PEC error occurs This bit can be set to 1 by hardware when the received PEC value does not match the value of PEC register. A NACK will be transmitted automatically when wrong PEC is received. This bit can be cleared by software by setting PECECLR bit; and be cleared by hardware when I2CEN=0. If SMBus mode is not supported, this bit will be reserved and be forced to 0 by hardware.
12	TTEFLG	R	Timeout or Tlow Error Flag 0: No timeout error 1: Timeout error occurs This bit can be set to 1 by hardware when timeout or external clock timeout occurs; be cleared by software by setting TTECLR bit; and be cleared by hardware when I2CEN=0. If SMBus mode is not supported, this bit will be reserved and be forced to 0 by hardware.
13	SMBALTFLG	R	SMBus Alert Occur Flag 0: No SMBus alarm 1: SMBus alarm occurred This bit can be set to 1 by hardware if HADDREN=1 (configured by SMBus HOST) and ALTEN=1, and SMBALERT falling edge is detected on SMBALERT pin; be cleared by software by setting SMBALTCLR bit; and be cleared by hardware when I2CEN=0. If SMBus mode is not supported, this bit will be reserved and be forced to 0 by hardware.
14	Reserved		
15	BUSBSYFLG	R	Bus Busy Flag 0: The bus is idle (no communication) 1: The bus is busy (in the progress of communication) This bit can be set to 1 by hardware when a start bit is detected; be cleared by hardware when a stop bit is detected; or be cleared when I2CEN=0.
16	TXDIRFLG	R	Transfer Direction Flag Update when the address matching event occurs. 0: Write transmission; the slave enters the receiving mode. 1: Read transmission; the slave enters the transmit mode.
23:17	ADDRCMFLG	R	Address Code Match Flag The received address is updated when the address match event occurs. 0: The address code does not match 1: The address code matches In 10-bit address, ADDRCMFLG provides the address after the first two bits of 10-bit address.
31:24	Reserved		

22.7.8 Interrupt flag clear register (I2C_INTFCLR)

Offset address: 0x1C

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	Reserved		
3	ADDRMCLR	W	Slave Address Match Flag Clear Set this bit, and the ADDRMFLG flag bit of I2C_STS register and START bit of I2C_CTRL2 register will be cleared. 0: Invalid operation 1: Clear ADDRMFLG and START
4	NACKCLR	W	Receive Not Acknowledge Flag Clear Set this bit and NACKFLG flag bit of I2C_STS register will be cleared. 0: Invalid operation 1: Clear NACKFLG
5	STOPCLR	W	Stop Bit Detection Flag Clear Set this bit and STOPFLG flag bit of I2C_STS register will be cleared. 0: Invalid operation 1: Clear STOPFLG
7:6	Reserved		
8	BERRCLR	W	Bus Error Flag Clear Set this bit and BERRFLG flag bit of I2C_STS register will be cleared. 0: Invalid operation 1: Clear BERRFLG
9	ALCLR	W	Arbitration Lost Flag Clear Set this bit and ALFLG flag bit of I2C_STS register will be cleared. 0: Invalid operation 1: Clear ALFFLG
10	OVRURCLR	W	Overrun/Underrun Flag Clear Set this bit and OVRURFLG flag bit of I2C_STS register will be cleared. 0: Invalid operation 1: Clear OVRURFLG
11	PECECLR	W	PEC Error in Reception Flag Clear Set this bit and PECEFLG flag bit of I2C_STS register will be cleared. 0: Invalid operation 1: Clear PECEFLG It SMBus mode is not supported, this bit will be reserved and be forced to 0 by hardware.
12	TTECLR	W	Timeout or Tlow Error Flag Clear Set this bit and TTEFLG flag bit of I2C_STS register will be cleared. 0: Invalid operation 1: Clear TTECLR It SMBus mode is not supported, this bit will be reserved and be forced to 0 by hardware.

Field	Name	R/W	Description
13	SMBALTCLR	W	SMBus Alert Occur Flag Clear Set this bit and SMBALTFLG flag bit of I2C_STS register will be cleared. 0: Invalid operation 1: Clear SMBALTFLG It SMBus mode is not supported, this bit will be reserved and be forced to 0 by hardware.
31:14	Reserved		

22.7.9 PEC register (I2C_PEC)

Offset address: 0x20

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	PEC	R	PEC Value Setup When PECEN=1, this bit field means the internal PEC value. This bit can be cleared by hardware when I2CEN=0.
31:8	Reserved		

22.7.10 Receive data register (I2C_RXDATA)

Offset address: 0x24

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	RXDATA	R	8-Bit Receive Data Byte Data byte received from I2C bus.
31:8	Reserved		

22.7.11 Transmit data register (I2C_TXDATA)

Offset address: 0x28

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	TXDATA	R/W	8-Bit Transmit Data Byte Data byte to be transmitted to I2C bus. This bit field can be set only when TXBEFLG=1.
31:8	Reserved		

23 Serial Peripheral Interface (SPI)

23.1 Full Name and Abbreviation Description of Terms

Table 76 Full Name and Abbreviation Description of SPI Terms

Full name in English	English abbreviation
Most Significant Bit	MSB
Least Significant Bit	LSB
Master Out Slave In	MOSI
Master In Slave Out	MISO
Serial Clock	SCK
Serial Data	SD
Master Clock	MCK
Word Select	WS
Pulse-code Modulation	PCM
Transmit	TX
Receive	RX
Busy	BSY

23.2 Introduction

Serial peripheral interface (SPI) provides data transmitting and receiving functions based on SPI protocol, which allows chips to communicate with external devices in half duplex, full duplex, synchronous and serial modes, and can work in master or slave mode.

23.3 Main Characteristics

（1） Master and slave operation with 3-wire full duplex synchronous transmission and receiving

（2） Simplex synchronous transmission can be realized by two wires (the third bidirectional data line can be included/not included)

（3） Select 8-bit or 16-bit transmission frame format

（4） Support multiple master device mode

（5） Support special transmission and receiving mark and can trigger interrupt

（6） Have SPI bus busy state flag

（7） SPI supports Motorola mode

（8） Fast communication in master/slave mode, up to 18MHz

（9） Clock polarity and phase are programmable

（10） Data sequence is programmable; select MSB or LSB first

（11） Interrupt can be triggered by master mode fault, overrun and CRC error flag

（12） Have DMA transmit and receive buffers

（13） Calculation, transmission and verification can be conducted through hardware CRC

（14） CRC error flag

（15） Two 32-bit embedded RXFIFO and TXFIFO have DMA function

23.4 Functional Description

23.4.1 Description of SPI Signal Line

Table 77 SPI Signal Line Description

Pin name	Description
SCK	Master device: SPI clock outputs Slave device: SPI clock inputs
MISO	Master device: Input the pin and receive data Slave device: Output the pin and send data Data direction: From slave device to master device
MOSI	Master device: Output the pin and send data Slave device: Input the pin and receive data Data direction: From master device to slave device
NSS	Software NSS mode: NSS pin can be used for other purposes. Hardware NSS mode of master device: NSS outputs, in single-master mode, NSS OFF output: Operation of multiple master environments is allowed, Slave hardware NSS mode: The NSS signal is set to low level as the chip selection signal of the slave

23.4.2 Communication format

In SPI communication, receiving data and transmitting data can be carried out at the same time. SCK sends and samples the data on the data line synchronously. The communication format depends on the clock phase, clock polarity and data frame format. If the communication is normal, the master device and the slave device must have the same communication format.

23.4.2.1 Phase and polarity of clock signal

The clock polarity and clock phase are CPOL and CPHA bits of SPI_CTRL1 register.

Clock polarity CPOL means the level signal of SCK signal line when SPI is in idle state.

- When CPOL=0, SCK signal line is in idle state and at low level
- When CPOL=1, SCK signal line is in idle state and at high level

Clock phase CPHA means the sampling moment of data

- When CPHA=0, the signal on MOSI or MISO data line will be sampled by the "odd edge" on SCK clock line.
- When CPHA=1, the signal on MOSI or MISO data line will be sampled by the "even edge" on SCK clock line.

SPI can be divided into four modes according to the states of clock phase CPHA and clock polarity CPOL.

Table 78 Four Modes of SPI

SPI mode	CPHA	CPOL	Sampling moment	Idle SCK clock
0	0	0	Odd edge	Low level
1	0	1	Odd edge	High level
2	1	0	Even edge	Low level
3	1	1	Even edge	High level

Note:

（1）To change CPOL and CPHA bits, SPI must be cleared and disabled through SPIEN bit

（2）When SCK is in idle state, if CPOL=1, pull up SCK; if CPOL=0, pull up SCK.

23.4.2.2 Data frame format

Select LSB or MSB first by configuring LSBSEL bit of SPI_CTRL1 register. Select the data word length by configuring DSCFG bit of SPI_CTRL2 register; no matter which data word length is selected; it must be aligned with FRTCFG when read access is conducted to FIFO. When accessing SPI_DATA register, the data frames are always right aligned. In the process of communication, only the bits within the data word length range will be output with the clock.

23.4.3 NSS mode

Software NSS mode: Select to enable or disable this mode by configuring SSEN bit of SPI_CTRL1 register, and the internal NSS signal level is driven by ISSEL bit of SPI_CTRL1 register.

Hardware NSS mode:

- Turn on NSS output: When SPI is in master mode, enable SSOEN bit, NSS pin will be pulled to low level and SPI will automatically enter the slave mode.
- Turn off NSS output: Operation is allowed in multiple master environments.

23.4.4 SPI mode

23.4.4.1 Initialization of SPI master mode

In master mode, serial clock is generated on SCK pin.

Configure master mode

- Configure MSMCFG=1 in SPI_CTRL1 register, and set it as master mode
- Select the serial clock baud rate by configuring BRSEL bit in SPI_CTRL1 register
- Select the polarity and phase by configuring CPOL and CPHA bits in SPI_CTRL1 register

- Select the transmission mode by configuring RXOMEN, BMOEN and BMEN bits in SPI_CTRL1 register
- Select the data bit width by configuring DSCFG bit in SPI_CTRL2 register
- Turn on NSS pulse mode by configuring NSSPEN bit in SPI_CTRL2 register (when configuring this bit, CPHA bit must be set to 1)
- Set RXFIFO threshold value for trigging RXBNEFLG event by configuring FRTCFG bit in SPI_CTRL2 register
- If DMA function is used, it is required to configure LDTX and LDRX bits of SPI_CTRL2 register
- If CRC is used, it is required to set CRC polynomial as input and also set CRCEN bit
- Select LSB or MSB first by configuring LSBSEL in SPI_CTRL1 register
- NSS configuration:
  - NSS pin works in input mode: in hardware mode, it is required to connect NSS pin to high level during the entire data frame transmission; in software mode, it is required to set SSEN bit and ISSEL bit in SPI_CTRL1 register
  - NSS works in output mode and it is required to configure SSOEN bit of SPI_CTRL2 register
- Configure SPIEN bit in SPI_CTRL1 register to enable SPI

In master mode: MOSI pin is data output, while MISO is data input.

23.4.4.2 Initialization of SPI slave mode

In slave mode, SCK pin receives the serial clock transmitted from the master device.

Configuration of slave mode

- Configure MSMCFG=0 in SPI_CTRL1 register, and set it as slave mode
- Select the polarity and phase by configuring CPOL and CPHA bits in SPI_CTRL1 register
- Select the transmission mode by configuring RXOMEN, BMOEN and BMEN bits in SPI_CTRL1 register
- Select the data bit width by configuring DSCFG bit in SPI_CTRL2 register
- Turn on NSS pulse mode by configuring NSSPEN bit in SPI_CTRL2 register (when configuring this bit, CPHA bit must be set to 1)
- Set RXFIFO threshold value for trigging RXBNEFLG event by configuring FRTCFG bit in SPI_CTRL2 register
- If DMA function is used, it is required to configure LDTX and LDRX bits of SPI_CTRL2 register
- If CRC is used, it is required to set CRC polynomial as input and also set CRCEN bit
- Select LSB or MSB first by configuring LSBSEL in SPI_CTRL1 register
- NSS configuration:
  - In hardware mode: NSS pin must be at low level in the whole data frame transmission process
  - In software mode: Set SSEN bit in SPI_CTRL1 register and clear ISSEL bit
- Configure SPIEN bit in SPI_CTRL1 register to enable SPI

In slave mode: MOSI pin is data input, while MISO is data output.

23.4.4.3 Full duplex communication of SPI

Usually, SPI is configured as full duplex communication, and the shift registers of

the master and the slave are connected through two unidirectional lines MOSI and MISO. During SPI communication, synchronous data transmission is conducted according to SCK clock edge. The data of the master are transmitted to the slave through MOSI pin, and the data of the slave are transmitted to the master through MISO pin. When the data transmission is completed, it means that the information is exchanged successfully.

23.4.4.4 Half-duplex communication of SPI

One clock line and one bidirectional data line

- Enable this mode by setting BMEN bit of SPI_CTRL1 register
- Control the data line to be input or output by setting BMOEN bit of SPI_CTRL1 register
- SCK pin is used as clock, MOSI pin is used in master device to transmit data, and MISO pin is used in slave device to transmit data

23.4.4.5 Simplex communication of SPI

One clock line and one unidirectional data line (receive-only or send-only)

In this mode, SPI mode is used as receive-only or send-only.

Send-only mode:

- Data are transmitted on send pin (MOSI in master mode, MISO in slave mode)
- Then the receive pin can be used as general-purpose I/O (MISO in master mode, MOSI in slave mode)

Receive-only mode:

- Turn off SPI output function by setting RXOMEN bit in SPI_CTRL1 register
- Release the send pin (MOSI in master mode, MISO in slave mode)
- In master mode, enable SPI to start communication, clear SPIEN bit of SPI_CTRL1 register and receiving data can be stopped immediately, not needing to read BSYFLG flag (always 1)
- In slave mode: Pull NSS to low level, and as long as SCK is pulsed by clock, SPI will always receive

23.4.4.6 Communication of multiple slave devices of SPI

SPI can be operated by multiple slave devices. The master device uses GPIO pin to manage the chip selection line of the slave device, and can control two or more independent slave devices.

The master device decides using which slave device to transmit data by pulling down the NSS pin of the slave device.

23.4.5 Data Transmitting and Receiving Process in Different SPI Modes

Table 79 Run Mode of SPI

Mode	Configure	Data pin
Full duplex mode of master device	BMEN=0，RXOMEN=0	MOSI sends; MISO receives
Unidirectional receiving mode of master device	BMEN=0，RXOMEN=1	MOSI is not used; MISO receives
Bidirectional transmitting mode of master device	BMEN=1，BMOEN=1	MOSI sends; MISO is not used
Bidirectional receiving mode of master device	BMEN=1，BMOEN=0	MOSI is not used; MISO receives

Mode	Configure	Data pin
Full duplex mode of slave device	BMEN=0，RXOMEN=0	MOSI receives; MISO transmits
Unidirectional receiving mode of slave device	BMEN=0，RXOMEN=1	MOSI receives; MISO is not used
Bidirectional transmitting mode of slave device	BMEN=1，BMOEN=1	MOSI is not used; MISO transmits
Bidirectional receiving mode of slave device	BMEN=1，BMOEN=0	MOSI receives; MISO is not used

Figure 96 Connection in Full Duplex Mode

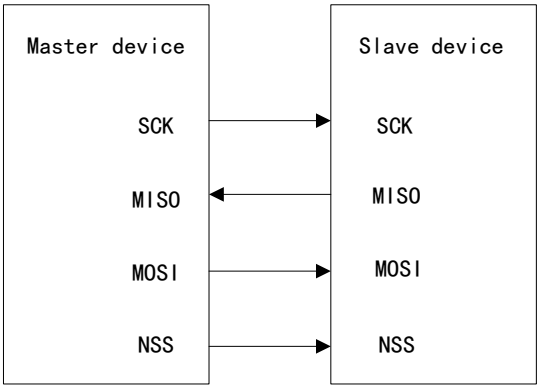


Figure 97 Connection in Simplex Mode (the master is used for receiving, while the slave is used for transmitting)

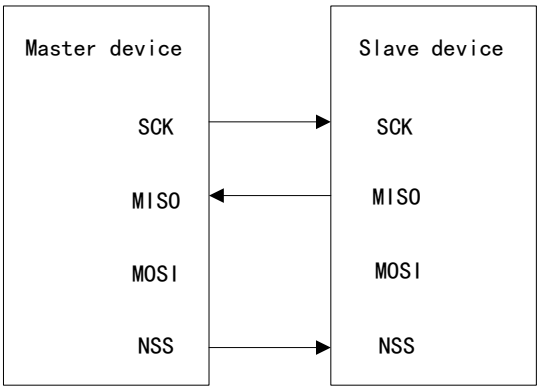


Figure 98 Connection in Simplex Mode (the master only transmits, while the slave receives)

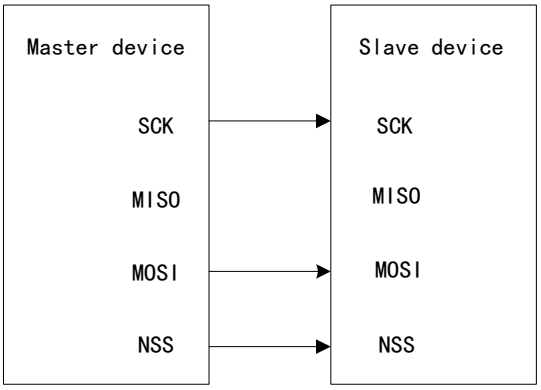
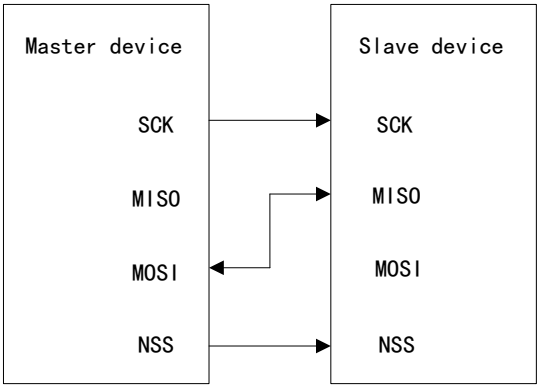


Figure 99 Connection in Half Duplex Mode



23.4.5.1 Transmitting and receiving of data

In order to prevent overrun when the data frame is short and ensure that SPI can work continuously, all SPI data need to pass through the 32-bit embedded FIFO. Each direction will have its own FIFO, TXFIFO and RXFIFO.

Handle FIFO according to SPI simplex and duplex mode, data frame format, access size executed on FIFO data register and whether to use data package to process FIFO when accessing FIFO.

After read access to SPI_DATA register, the earliest values that have not been read yet and are stored in RXFIFO will be returned. After write access to SPI_DATA, the written data will be stored in TXFIFO at the end of the transmit queue. Read access must always be aligned with RXFIFO threshold value configured by FRTCFG bit in SPI_CTRL2 register. The FTLSEL and FRLSEL bits indicate the current occupancy levels of the two FIFOs.

The read access to SPI_DATA register must be managed by RXBNEFLG event. When the data are stored in RXFIFO and reach the threshold value (defined by previous bit), this event will be triggered; when RXBNEFLG is cleared, RXFIFO will be regarded to be empty, and in the similar way, the write access to the data frame to be transmitted is managed by TXBEFLG event. When TXFIFO is less than or equal to half its capacity, RXBNEFLG event will be triggered; otherwise, TXBEFLG will be cleared, meanwhile, it will be regarded that there are data stored in TXFIFO. Therefore, when the data frame format is less than or equal to one byte, RXFIFO can store 4 data frames at most, and TXFIFO can store 3 data frames. When the software attempts to write more data to TXFIFO in 16-bit mode, this difference can prevent the three or eight data frames that have been stored in TXFIFO from being damaged. TXBEFLG and RXBNEFLG events can be polled or handled by interrupt.

23.4.5.2 Sequence processing

In transmitting data, multiple data can be formed into a sequence in order. When the transmission is started, TXFIFO will send continuously in order.
In single receive mode, in half duplex or simplex mode, when SPI is enabled, the master device will immediately receive the sequence until SPI is off or the single receive mode is off. When the data frame starts transmission, the slave cannot control the data sequence, so the slave must prepare the data before the transmission, to ensure there are data to be transmitted in TXFIFO.

When there are multiple slave devices, each sequence needs to be corresponding to different slave devices, so NSS pulse should be used to separate the sequence to ensure it is correct.

Note:

（1） Check whether the data transmission is completed according to FTLSEL bit and BSYFLG bit, and the clock output will stop when the transmission is completed.

（2） In packet mode, special attention should be paid to empty bytes when the data being transmitted are odd.

（3） In single receive mode, the master device needs to disable SPI or single receive mode to stop clock output.

（4） Master the correct receiving time to ensure the correct data transmission

（5） The action of closing should be between the sampling time of first bit and the first bit of the next byte.

23.4.5.3 Data packing

If the data frame is less than or equal to one byte, when executing 16-bit read and write access to SPI_DATA register, the data will be packed automatically and double data can be processed in parallel. After conducting write access to SPI_DATA, 2-byte data will be transmitted; if the threshold value of RXFIFO is set to 16 bits, a receive RXBNEFLG event will be generated.

For a single RXBNEFLG event, the data receiver will perform one read operation to SPI_DATA, and only after that, can it obtain all data.

Note: The threshold value of RXFIFO should be consistent with the bit width of follow-up data access.

23.4.6 NSS Pulse Mode

NSS pulse mode can be set by configuring NSSPEN bit of SPI_CTRL1 register; this mode take effect only when SPI is configured as Motorola master mode and captures the first edge. In transmitting of this mode, NSS pulse is generated between two continuous data frames, and NSS will remain high for at least one cycle. NSS pulse mode allows the slave to latch data.

23.4.7 TI Mode

Master mode of TI protocol

SPI interface can be made compatible with master mode of TI protocol by configuring FRFCFG bit of SPI_CTRL2 register.

In master mode of TI protocol, it is unaffected by the setting of SPI_CTRL1 register, and the clock polarity, phase and NSS management will meet the requirements of TI protocol. In slave mode, SPI baud rate frequency divider is used to control MISO pin to make MISO pin to be in high-impedance state, and any baud rate can be used to ensure the best flexibility.

Generally the baud rate is set as the baud rate of external master clock, and the delay for MISO signal to become the high-impedance state depends on the baud rate set synchronously and through BRSEL bit of SPI_CTRL1 register internally. The formula is:

$$T_{baud\_rate}/2+4\times t_{pclk}<t_{release}<t_{baud\_rate}+6\times t_{pclk}$$

Note: This function does not apply to Motorola SPI communication mode (FRFCFG bit is set to 0)

23.4.8 CRC Functions

SPI module contains two CRC computing units, which are used for data receiving and data transmission respectively.

CRC computing units are used to define polynomials in SPI_CRCPOLY register (it should be odd, and does not support even number).

Enable CRC computing by configuring CRCEN bit in SPI_CTRL1 register; at the same time, reset the CRC register (SPI_RXCRC and SPI_TXCRC).

CRC is managed by CPU during transmission

To obtain the CRC value of transmission calculation, after the last data is written to the transmit buffer, it is required to set CRCNXT bit of SPI_CTRL1; indicate that the hardware sends the CRC value after the last data is transmitted, and the CRCNXT bit will be cleared; during CRC data transmission, CRC computing will be frozen.

The received CRC data will be stored in RXFIFO. A CRC transaction usually needs one more data frame to communicate at the end of the data sequence. However, when an 8-bit data frame checked by 16-bit CRC is set, two data frames are needed to send the complete CRC. When the last CRC data is received, the received value and the value of SPI_RXCRC register will be compared. By checking CRCEFLG flag bit in SPI_STS register, judge whether the data are damaged in the process of transmission. CRCEFLG bit can be cleared by writing 0. RXBNEFLG bit can be cleared by reading SPI_DATA register.

Sequence of clearing CRC values

（1） Disable SPI (SPIEN=0)

（2） Clear CRCEN bit

（3） Set CRCEN bit to 1

（4） Enable SPI (SPIEN=1)

Note: When SPI works in slave mode, the software must enable CRC operation when the clock is stable. And in the data phase and CRC phase, the NSS signal needs to be pulled down and maintained.

23.4.9 DMA Function

For high-speed data transmission, the request/response DMA mechanism in SPI improves the system efficiency and can transfer data to SPI transmit buffer promptly, and the receive buffer can read the data in time to prevent overflow.

When SPI only sends data, it is only needed to enable DMA transmission channel.When SPI only receives data, it is only needed to enable DMA receiving channel.

DMA function of SPI mode can be enabled by configuring TXDEN and RXDEN bits of SPI_CTRL2 register.

- When transmitting: When TXBEFLG flag bit is set to 1, issue the DMA request, DMA controller writes data to SPI_DATA, and then the TXBEFLG flag bit will be cleared.
- When receiving: When setting RXBNEFLG flag bit to 1, issue the DMA request, DMA controller reads data from SPI_DATA register, and then RXBNEFLG flag bit is cleared.

By monitoring BSYFLG flag bit, confirm whether SPI communication is over after DMA has transferred all data to be transmitted in transmit mode, which can avoid damaging the transmission of last data.

DMA function with CRC

By the end of communication, if SPI enables both CRC operation and DMA function, transmitting and receiving of CRC bytes will be completed automatically. The CRCNXT bit is not controlled by software. The transmitting DMA channel counter of SPI must be set to the number that does not contain CRC data, but the DMA channel counter must contain the length of one more CRC data when receiving.

After reading CRC data in CRC check link, the values of SPI_TXCRC and SPI_RXCRC will be cleared automatically. Then continuous transmission can be realized by DMA circular mode (except in single receive mode).

At the end of data and CRC transmission, if CRCEFLG flag bit of SPI_STS register is set to 1, it indicates that an error occurred during transmission.

23.4.10 SPI disable

After data transmission is over, end the communication by closing SPI module.

When data are being transmitted or there are data in TXFIFO, it is not allowed to turn off SPI by operating SPIEN bit in SPI_CTRL1 register. If SPIEN=0 is set, the clock signal will be transmitted continuously until the peripheral is enabled again. Certain steps are required to turn off SPI in order to prevent the above situations.

Steps of turning off SPI

（1） Wait for clearing FTLSEL

（2） Wait for clearing BSYFLG flag bit

（3） Wait for clearing FRLSEL

（4） Disabe SPI (SPIEN=0)

Steps of turning off SPI in some single receive mode

（1） Wait for clearing RXOMEN or setting BMOEN to 1

（2） Wait for clearing BSYFLG flag bit

（3） Wait for clearing FRLSEL

（4） Disable SPI (SPIEN=0)

23.4.11 SPI interrupt

An interrupt can be triggered by the following events during SPI operation:

- TXFIFO prepares for loading
- RXFIFO receives data
- Master mode error
- CRC error
- TI frame format error

23.4.11.1 State flag bit

There are three flag bits for fully monitoring the state of SPI bus

Transmit buffer empty flag TXBEFLG

TXBEFLG=1 means that TXFIFO has space to store the transmitted data; TXBEFLG flag bit is connected to TXFIFO bit, and in the process of storing data, if the storage content of TXFIFO is less than or equal to FIFO/2, TXBEFLG flag bit is kept high. When the storage content of TXFIFO is greater than FIFO/2, TXBEFLG flag bit will be cleared. If TXBEIEN bit in SPI_CTRL2 register is set, an interrupt will be generated.

Receive buffer non-empty flag RXBNEFLG

RXBNEFLG flag bit depends on the value of FRTCFG bit in SPI_CTRL2 register:

- If FRTCFG=1, when the storage content of RXFIFO is greater than or equal to 8 bits, RXBNEFLG=1
- If FRTCFG=0, when the storage content of RXFIFO is greater than or equal to 16 bits, RXBNEFLG=1

RXBNEFLG flag bit will be cleared automatically if not in the above situations.

If RXBNEIEN=1 in SPI_CTRL2 register, an interrupt will be generated.

Busy flag BSYFLG

BSYFLG flag is set and cleared by hardware, which can indicate the state of SPI communication layer. When BSYFLG=1, it indicates SPI is communicating. BSYFLG flag can be used to detect whether transmission is over to avoid damaging the last transmitted data.

BSYFLG flag will be cleared in the following situations

- End the transmission in master mode
- Master mode fault
- In slave mode, there is at least one SPI cycle between two data transmissions
- Disable SPI

During continuous communication:

- In master mode: BSYFLG=1 in the whole transmission process
- In save mode: BSYFLG is kept low within one SCK clock cycle between transmission of each data

Note: It is best to use TXBEFLG and RXBNEFLG flags to process the transmitting and receiving of each data item

23.4.11.2 Error flag bit

Master mode error MEFLG

MEFLG is an error flag bit.

The master mode error occurs when:

- in hardware NSS mode, the NSS pin of the master device is pulled down
- in software NSS mode, ISSEL bit is cleared
- MEFLG bit is set automatically

Effect of master mode failure:

- MEFLG is set to 1, and if ERRIEN is set, SPI interrupt will be generated
- SPIEN is cleared (output stops, SPI interface is disabled)
- MSMCFG is cleared and the device is forced to enter the slave mode

Operation of clearing the MEFLG flag bit:

- When MEFLG flag bit is set to 1, it is required to read or write SPI_STS register, and then write to SPI_CTRL1 register.
- When MEFLG flag bit is 1, it is not allowed to set SPIEN and MSMCFG bits.

Overrun error OVRFLG

An overrun error will be generated when the following events occur

- When RXBNEFLG flag bit is still 1 after the master device has transmitted data
- When the space in RXFIFO cannot store the data to be received when receiving data
- When the software or DMA cannot read the data in RXFIFO in time
- When CRC is only enabled in receiving mode, RXFIFO is not available and the receive buffer is limited to the single data frame buffer

When an overrun error occurs: OVRFLG bit is set to 1; if ERRIEN bit is also set, an interrupt will be generated.

After an overrun error occurs, the data in the receiving buffer are not the data transmitted by the master device, and by reading SPI_DATA value, the data are the data not read before, and the subsequent data will be discarded.

OVRFLG flag can be cleared by reading SPI_DATA register and SPI_STS register according to the sequence.

CRC error flag bit CRCEFLG

Enable CRC operation by setting CRCEN bit of SPI_CTRL1 register, and CRC error flag can check whether the received data are valid.

When the value transmitted by SPI_TXCRC register does not match the value in SPI_RXCRC register, a CRC error will be generated, and CRCEFLG flag bit in SPI_STS register will be set to 1.

CRCEFLG can be cleared by writing 0 to CRCEFLG bit of SPI_STS register.

TI mode frame format error (FREFLG)

Under the slave device and in accordance with TI mode protocol, when a pulse appears in NSS during data communication, a TI mode frame format error will be caused. When TI mode frame format error occurs, FREFLG flag bit of SPI_STS register will be set to 1, SPI will not be disabled, NSS pulse will be ignored, and SPI will wait for the next NSS pulse before retransmission. As the error detection may cause the loss of two data bytes, the data may have been damaged.

FREFLG flag can be cleared by reading SPI_STS register. If ERRIEN bit is set, an interrupt will be generated when NSS error occurs. At this time, SPI is disabled because the consistency of data cannot be guaranteed. When SPI is enabled again, the master server needs to be reinitialized.

Table 80 SPI Interrupt Request

Interrupt flag	Interrupt event	Enable control bit	Clearing method
TXBEFLG	Transmit buffer empty flag	TXBEIEN	Write SPI_DATA register
RXBNEFLG	Receive buffer non-empty flag	RXBNEIEN	Read SPI_DATA register
MEFLG	Master mode failure event flag	ERRIEN	Read/Write SPI_STS register and then write SPI_CTRL1 register
OVRFLG	Overrun error flag		Read SPI_DATA register and then read SPI_STS register
CRCEFLG	CRC error flag		Write 0 to CRCEFLG bit
FREFLG	TI mode frame format error flag		Read SPI_STS register

23.5 Register Address Mapping

Table 81 SPI Register Address Mapping

Register name	Description	Offset address
SPI_CTRL1	SPI control register 1	0x00
SPI_CTRL2	SPI control register 2	0x04
SPI_STS	SPI state register	0x08
SPI_DATA	SPI data register	0x0C
SPI_CRCPOLY	SPI CRC polynomial register	0x10
SPI_RXCRC	SPI receive CRC register	0x14
SPI_TXCRC	SPI transmit CRC register	0x18

23.6 Register Functional Description

These peripheral registers can be operated by half word (16 bits) or word (32 bits).

23.6.1 SPI control register 1 (SPI_CTRL1)

Offset address: 0x00

Reset value: 0x0000

Field	Name	R/W	Description
0	CPHA	R/W	Clock Phase Configure This bit indicates on the edge of which clock to start sampling 0: On the edge of the frist clock 1: On the edge of the second clock Note: This bit cannot be modified during communication.
1	CPOL	R/W	Clock Polarity Configure When SPI is in idle state, SCK will remain in level state. 0: Low level 1: High level Note: This bit cannot be modified during communication
2	MSMCFG	R/W	Master/Salve Mode Configure 0: Configure as slave mode 1: Configure as master mode Note: This bit cannot be modified during communication
5:3	BRSEL	R/W	Baud Rate Divider Factor Select 000：DIV=2 001：DIV=4 010：DIV=8 011：DIV=16 100：DIV=32 101：DIV=64 110：DIV=128 111：DIV=256 Baud rate=FPCLK/DIV Note: This bit cannot be modified during communication
6	SPIEN	R/W	SPI Device Enable 0: Disable 1: Enable Note: When SPI device is disabled, please operate according to the process of disabling SPI.
7	LSBSEL	R/W	LSB First Transfer Select 0: First send the most significant bit (MSB) 1: First send the least significant bit (LSB)
8	ISSEL	R/W	Internal Slave Device Select When SSEN=1 (software NSS mode), select internal NSS level by configuring the bit 0: Internal NSS is low 1: Internal NSS is high
9	SSEN	R/W	Software Slave Device Enable 0: Software NSS mode is disabled, and the internal NSS level is determined by external NSS pin 1: Software NSS mode is enabled, and the internal NSS level is determined by ISSEL value.
10	RXOMEN	R/W	Receive Only Mode Enable 0: Transmit and receive at the same time

Field	Name	R/W	Description
			1: Receive-only mode RXOMEN bit and BMEN bit together determine the transmission direction in the two-line and two-way mode. In the configuration of multiple slave devices, in order to avoid data transmission conflict, it is necessary to set RXOMEN bit to 1 on the slave devices that are not accessed.
11	CRCLSEL	R/W	CRC Length Select 0: Use 8-bit CRC 1: Use 16-bit CRC Note: Only when SPIEN=0, can CRC error be changed.
12	CRCNXT	R/W	CRC Transfer Next Enable 0: Next value to be transmitted is from transmit buffer 1: Next value to be transmitted is from transmit CRC register Note: After the last data is written to SPI_DATA register, set CRCNXT bit immediately.
13	CRCEN	R/W	CRC Calculate Enable 0: CRC check is disabled 1: CRC check is enabled CRC check function only applies to full duplex mode; only when SPIEN=0, can this bit be changed.
14	BMOEN	R/W	Bidirectional Mode Output Enable 0: Disable (receive-only ode) 1: Enable (send-only mode) When BMEN=1, namely in single-line bidirectional mode, this bit determines the transmission direction of the transmission line.
15	BMEN	R/W	Bidirectional Mode Enable 0: Double-line unidirectional mode 1: Single-line bidirectional mode Single-line bidirectional transmission means: transmission between MOSI pin of data master and MISO pin of slave.

23.6.2 SPI control register 2 (SPI_CTRL2)

Offset address: 0x04

Reset value: 0x0700

Field	Name	R/W	Description
0	RXDEN	R/W	Receive Buffer DMA Enable When RXDEN=1, once RXBNEFLG flag is set, DMA request will be issued. 0: Disable 1: Enable
1	TXDEN	R/W	Transmit Buffer DMA Enable When this bit is set, once TXBEFLG flag is set, DMA request will be issued. 0: Disable 1: Enable
2	SSOEN	R/W	SS Output Enable SS output in master mode 0: SS output is disabled, and it can work in multi-master mode. 1: SS output is enabled, and it cannot work in multi-master mode.

Field	Name	R/W	Description
			Note: Not available in TI mode of SPI.
3	NSSPEN	R/W	NSS Pulse Management Enable 0: Disable 1: Enable Note: (1) During continuous transmission, it is allowed to generate NSS pulse between transmission of two data. (2) During single data transmission, NSS pin will be forced to be pulled up at the end of transmission. (3) This bit is invalid when CPHA=1 or FRFCFG=1. (4) This bit can be written only when SPIEN=0. (5) Not available in TI mode of SPI.
4	FRFCFG	R/W	Frame Format Configure 0: SPI Motorola mode 1: SPI TI mode Note: This bit can be written only when SPIEN=0.
5	ERRIEN	R/W	Error interrupt Enable 0: Disable 1: Enable When an error occurs, ERRIEN bit controls whether to generate the interrupt.
6	RXBNEIEN	R/W	Receive Buffer Not Empty Interrupt Enable 0: Disable 1: Allowe When RXBNEFLG flag bit is set to 1, an interrupt request will be generated
7	TXBEIEN	R/W	Transmit Buffer Empty Interrupt Enable 0: Disable 1: Enable When TXBEFLG fag bit is set to 1, an interrupt request will be generated
11:8	DSCFG	R/W	Data Size Configure Configure the bit width of SPI transmission date: 0000: Reserved 0001: Reserved 0010: Reserved 0011: 4 bits 0100: 5 bits 0101: 6 bits 0110: 7 bits 0111: 8 bits 1000: 9 bits 1001: 10 bits 1010: 11 bits 1011: 12 bits 1100: 13 bits 1101: 14 bits 1110: 15 bits 1111: 16 bits Note: When reserved bit is written by software, the value will be forced to be 0111 (8 bits).
12	FRTCFG	R/W	FIFO Reception Threshold Configure Configure FIFO threshold, and when the value exceeds this threshold, RXBNEFLG will occur 0: 16 bits

Field	Name	R/W	Description
			1: 8 bits
13	LDRX	R/W	Last DMA Receive These bits are used in data packing mode to define the total number received by DMA to be odd or even. 0: Even 1: Odd Note: (1) These bits are meaningful only when RXDEN bit of SPI_CTRL2 register is set and the packing mode is enabled. (2) This bit can be written only when SPIEN=0. (3) To disable the SPI, perform steps described in 23.4.10.
14	LDTX	R/W	Last DMA Transmit These bits are used in data packing mode to define the total number transmitted by DMA to be odd or even. 0: Even 1: Odd Note: (1) These bits are meaningful only when RXDEN bit of SPI_CTRL2 register is set and the packing mode is enabled. (2) This bit can be written only when SPIEN=0. (3) To disable the SPI, perform steps described in 23.4.10.
15	Reserved		

23.6.3 SPI state register (SPI_STS)

Offset address: 0x08

Reset value: 0x0002

Field	Name	R/W	Description
0	RXBNEFLG	R	Receive Buffer Not Empty Flag 0: Empty 1: Not empty
1	TXBEFLG	R	Transmit Buffer Empty Flag 0: Not empty 1: Empty
3:2	Reserved		
4	CRCEFLG	RC_W0	CRC Error Occur Flag This bit indicates whether the received CRC value matches the value of RXCRC register 0: Match 1: Not match This bit is set by hardware, and it can be cleared by writing 0 to this bit by software.
5	MEFLG	R	Mode Error Occur Flag 0: Not occur 1: Occurred This bit is set by hardware, and it can be cleared by writing 0 to this bit by software.
6	OVRFLG	R	Overrun Occur Flag 0: Not occur 1: Occurred This bit is set by hardware, and it can be cleared by writing 0 to this bit by software.
7	BSYFLG	R	SPI Busy Flag This bit indicates the work state of SPI 0: SPI is idle

Field	Name	R/W	Description
			1: SPI is communicating It is set or cleared by hardware.
8	FREFLG	R	Frame Format Error Flag 0: Not occur 1: Occurred Note: This bit is set to 1 by hardware and cleared when reading SPI_STS register.
10:9	FRLSEL	R	FIFO Receive Leve Select 00: FIFO is emty 01：FIFO/4 10：FIFO/2 11: FIFO is full Note: This bit is set to 1 and cleared by hardware. It is not used in SPI single receiving mode with CRC check.
12:11	FTLSEL	R	FIFO Transmit Leve Select 00: FIFO is emty 01：FIFO/4 10：FIFO/2 11: FIFO is full (it can be considered as full when the threshold value of FIFO is greater than 1/2) Note: This bit set 1 or clear 0 by hardware.
15:13	Reserved		

23.6.4 SPI data register (SPI_DATA)

Offset address: 0x0C

Reset value: 0x0000

Field	Name	R/W	Description
15:0	DATA	R/W	Transmit Receive Data register Store the data to be transmitted or received. When writing this register, the data will be written to the transmit buffer; when reading this register, the data in receive buffer will be read. The size of the buffer is consistent with the length of the data frame, that is, for 8-bit data, DATA[7:0] will be used when transmitting and receiving data, and DATA[15:8] is invalid; for 16-bit data, DATA[15:0] will be used when transmitting and receiving data.

23.6.5 SPI CRC polynomial register (SPI_CRCPOLY)

Offset address: 0x10

Reset value: 0x0007

Field	Name	R/W	Description
15:0	CRCPOLY	R/W	CRC Polynomial Value Setup This register contains CRC polynomial of CRC computing, which can be modified and the reset value is 0x0007.

23.6.6 SPI receive CRC register (SPI_RXCRC)

Offset address: 0x14

Reset value: 0x0000

Field	Name	R/W	Description
15:0	RXCRC	R	Receive Data CRC Value The CRC data of receive bytes calculated by hardware are stored in this register; the bits and the length of data frames are consistent, that is, if the received data are 8 bits, the CRC computing is made based on CRC8; if the received data are 16 bits, the CRC computing is made based on CRC16. When CRCEN is set, the hardware clears the register. Note: When BSYFLG bit is set to 1, the value of reading RXCRC register may be wrong.

23.6.7 SPI transmit CRC register (SPI_TXCRC)

Offset address: 0x18

Reset value: 0x0000

Field	Name	R/W	Description
15:0	TXCRC	R	Transmit Data CRC Value The CRC data of transmitted bytes calculated by hardware are stored in TXCRC; the bits and the length of data frames are consistent, that is, if the transmitted data are 8 bits, the CRC computing is made based on CRC8; if the transmitted data is are 16 bits, the CRC computing is made based on CRC16. When CRCEN is set, the hardware clears the register. Note: When BSYFLG bit is set to 1, the value of reading RXCRC register may be wrong.

24 Analog/Digital Converter (ADC)

24.1 Full Name and Abbreviation Description of Terms

Table 82 Full Name and Abbreviation Description of ADC Terms

Full name in English	English abbreviation
Analog watchdog	AWD
Conversion	C
Injected	INJ
Regular	REG
Start	S
Scan	SCAN
Single	SINGLE
Automatic	A
Group	G
Discontinuous	DISC
Count	CNT
Dual	DUAL
Continuous	C
Calibration	CAL
Reset	RST
Alignment	ALIGN
External	EXT
Event	E
Trigger	TRG
Temperature	T
Sensor	S
Time	TIM
Sample	SMP
Offset	OF
High	H
Low	L
Threshold	T
Sequence	SEQ

Full name in English	English abbreviation
Length	LEN
-	
Regular Channels	REG
Injected Channel	INJ
Injected Group	INJG
-	
Continuous Conversion	CONTC
Single Conversion	SINGLEC
External Trigger	EXTTRG
Sample Time	SMPTIM
Number	NUM

24.2 Introduction

This series of products has 1 ADC, the accuracy is 12 bits, Up to including 16 external channels and 2 internal channels, and there are single, continuous and intermittent A/D conversion modes for each channel. ADC conversion results can be left-aligned or right-aligned and stored in 16-bit data register.

24.3 Main Characteristics

（1） ADC power supply requirements: From 2.4V to 3.6V

（2） ADC input range: $V_{SSA} \leqslant V_{IN} \leqslant V_{DDA}$

（3） 12-bit resolution

（4） Conversion mode
- Single conversion mode
- Continuous conversion mode
- Discontinuous mode

（5） Analog input channel category
- External GPIO input channel
- One internal temperature sensor (V_{SENSE}) input channel
- One internal reference voltage (V_{REFINT}) input channel

（6） High performance
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution.
- Self-calibration
- Programmable sampling time
- Data alignment
- DMA supported trigger mode

（7） Low power

- Low-power operation reduces PCLK frequency and maintains optimum ADC performance
- Automatic delay mode: Run in PCLK low speed, to prevent ADC over-limit
- Automatic shutdown mode: ADC can power off automatically at other times except during conversion period

（8） Interrupt

- End of conversion interrupt
- End of sequence conversion interrupt
- End of sampling phase interrupt
- ADC ready interrupt
- Overrun interrupt
- Analog watchdog state reset interrupt

（9） Trigger mode

- External pin signal trigger
- Internal signal trigger generated by on-chip timer

24.4 Functional Description

24.4.1 ADC Pin and Internal Signal

Table 83 ADC Internal Signal

Name	Instruction	Signal type
TMRx_TRG	Internal information from timer	Input
V_{SENSE}	Output voltage of internal temperature sensor	Input
V_{REFINT}	Output of internal reference voltage	Input

Table 84 ADC Pins

Name	Instruction	Signal type
V_{DDA}	Analog power supply equivalent to V_{DD} and: 2.4V $\leqslant V_{DDA} \leqslant V_{DD}$(3.6V)	Input, analog power supply
V_{SSA}	Analog power equivalent to V_{SS}	Input, analog power ground
ADC_IN[15:0]	16 analog inputs channels	Analog input signal

24.4.2 Calibration

The function of calibration is to eliminate the offset error of A/D conversion of each chip, so calibration should be conducted before A/D conversion, and ADC module cannot be used during calibration.

Calibration configuration process:

- Configure ADCEN bit of register ADC_CTRL to 0, and disable ADC
- Configure CAL bit of register ADC_CTRL to 1, and enable calibration
- After calibration is completed, CAL bit is automatically cleared by hardware
- The calibration factor is read in CDATA[6:0] bit of register ADC_DATA

24.4.3 ADC Conversion Mode

24.4.3.1 Single conversion mode

In this mode, for single channel, only one conversion is performed for this channel, and for multiple channels, only one conversion is performed for this group of channels .

When CMODESEL bit of configuration register ADC_CFG1 is 0, ADC is set to single conversion mode; ADC conversion can be enabled by setting STARTCEN bit of configuration register ADC_CTRL to 1 by software or by trigger event of hardware.

After the conversion of each channel, the converted data will be stored in the 16-bit ADC_DATA register, EOCFLG bit will be set to 1, and if EOCIEN bit is set to 1, an interrupt will be generated. After the channel sequence conversion, EOSEQFLG bit will be set to 1, and if EOSEQIEN bit is set to 1, an interrupt will be generated.

24.4.3.2 Continuous conversion mode

In this mode, for single channel, continuous conversion is only conducted for this channel; for multiple channels, continuous conversion is only conducted for this group of channel.

When CMODESEL bit of register ADC_CFG1 is configured to 1, ADC is set to continuous conversion mode; configure STARTCEN bit of register ADC_CTRL to 1 by software or trigger the event by hardware to enable ADC conversion.

After the conversion of each channel, the converted data will be stored in the 16-bit ADC_DATA register, EOCFLG bit will be set to 1, and if EOCIEN bit is set to 1, an interrupt will be generated. After the channel sequence conversion, EOSEQFLG bit will be set to 1, and if EOSEQIEN bit is set to 1, an interrupt will be generated.

24.4.3.3 Discontinuous mode

Configure DISCEN bit of register ADC_CFG1 to 1, and set ADC to discontinuous mode; enable ADC conversion by software or by trigger event of hardware. In this mode, only one channel of one sequence is converted at a time. If DISCEN bit is cleared, all channels of one sequence will be converted at a time.

Example:

- DISCEN bit is set to 1, and the channel sequence is 0, 1, 5
  - 1st trigger, Channel 0 is converted and generates an EOCFLG event
  - 2nd trigger, Channel 1 is converted and generates an EOCFLG event
  - 3rd trigger, Channel 5 is converted and generates an EOCFLG event
- DISCEN bit is set to 0, and the channel sequence is 0, 1, 5
  - 1st trigger, Channels 0, 1 and 5 are converted in sequence. After the conversion of each channel, an EOCFLG event will be generated. After the conversion of the whole sequence, an EOSEQFLG event will be generated

24.4.4 ADC Channel Classification

24.4.4.1 Analog input channel introduced by GPIO pin

In total 16 channels are connected to ADC_IN0…ADC_IN15.

24.4.4.2 Internal analog input channel

Temperature sensor

（1） The temperature sensor is used to measure the internal temperature of the chip
（2） The temperature sensor selects ADC1_IN16 input channel
（3） Enable by TSEN bit of configuration register ADC_CCFG
（4） Select sampling time

Internal reference voltage V_{REFINT}

（5） The internal reference voltage is used to provide a stable voltage output for ADC
（6） Internal reference voltage V_{REFINT} is used to select ADC1_IN17 input channel

24.4.5 External Trigger and Trigger Polarity

Table 85 Configuration Trigger Polarity

EXTPOLSEL	Source
00	Detection of disabled trigger
01	Detection on rising edge
10	Detection on falling edge
11	Detection on both rising edge and falling edge

The external trigger event can be selected by EXTTRGSEL bit of configuration register ADC_CFG1.

When the bit EXTPOLSEL≠"0b00" for the register ADC_CFG1, the external event can trigger conversion on its selected polarity.

Table 86 External Trigger

Trigger source	EXTTRGSEL[2:0]	Trigger type
TMR1_TRGO	000	Internal signal from the on-chip timer
TMR1_CC4	001	
Reserved	010	
TMR3_TRGO	011	
TMR15_TRGO	100	
Reserved	101	
Reserved	110	
Reserved	111	External pin

24.4.6 Data Register

The data can be left-aligned or right-aligned, which is determined by DALIGCFG bit of configuration register ADC_CFG1 ADC conversion results can be left-aligned or right-aligned and stored in 16-bit data register.

24.4.7 Programmable Conversion Resolution

Reducing the resolution can improve the conversion time and 12, 10, 8 or 6-bit modes can be selected by DATARESCFG bit of configuration register ADC_CFG1.

Table 87 Conversion Time of tSAR Related to Conversion Resolution

DATARESCFG bit	t_{SAR}	t_{SAR} (ns)@f_{ADC}=14MHz	$t_{SMPL(min)}$	t_{ADC}	t_{ADC}(μs)@f_{ADC}=14MHz
6	7.5	535ns	1.5	9	643ns
8	9.5	678ns	1.5	11	785ns
10	11.5	821ns	1.5	13	928ns
12	12.5	893ns	1.5	14	1000ns

24.4.8 Interrupt

Table 88 ADC Interrupt

Interrupt event	Event flag	Enable control
End of conversion	EOCFLG	EOCIEN
End of sequence conversion	EOSEQFLG	EOSEQIEN
End of sampling phase	EOSMPFLG	EOSMPIEN
ADC ready	ADCRDYFLG	ADCRDYIEN
Overrun	OVREFLG	OVRIEN
Analog watchdog state reset	AWDFLG	AWDIEN

24.4.9 ADC Overrun

ADC overrun means when the converted data is not read by DMA or CPU on time, another converted data will take effect.

When EOCFLG bit is 1 but another new conversion has been completed, an overrun event will occur, and OVREFLG bit of register ADC_STS will be set to 1; if OVRIEN bit is set to 1, an overrun interrupt will be generated.

It is determined by OVRMAG bit of configuration register ADC_CFG1 that the data in the ADC data register are held or covered when an overrun event occurs:

- OVRMAG is 0: When an overrun event is detected, old data will be held in ADC_DATA register
- OVRMAG is set to 1: When an overrun event is detected, ADC_DATA register will cover the data by the last converted data

24.4.10 Data Conversion Management

24.4.10.1 No DMA participating in data conversion management

The software controls data conversion. Every time the conversion is completed, EOCFLG will be set to 1, and the conversion results will be read from ADC_DATA register. Then OVRMAG bit in ADC_CFG1 register should be 0.

24.4.10.2 No DMA and overrun participating in data conversion management

When one or more channels are converted and each conversion result does not need to be read, OVRMAG bit will be set to 1, overrun event cannot prevent ADC conversion and the register ADC_Data only saves the last converted data.

24.4.10.3 DMA management of data conversion

DMA transmission can be used to transmit the conversion results from the data register to the memory in time to prevent loss of the conversion results in the ADC_DATA register.

DMA can be enabled by setting DMAEN bit of the register ADC_CFG1 to 1. After each conversion, a DMA request will be generated to transmit the converted data of data register to the memory.

When DMA fails to respond to DMA request in time, an overrun event will be generated, and OVREFLG bit will be set to 1. After that, ADC will not generate DMA request and DMA will not transmit new conversion results. DMA will start to work again when OVREFLG bit is cleared.

DMA mode is selected by DMACFG bit of configuration register ADC_CFG1:

- When DMACFG is 0, DMA is in single mode
  - DMA programming is used to transmit the fixed-length data
  - In this mode, ADC will generate DMA request every time it converts data effectively. When ADC conversion is restarted, ADC will stop generating DMA request
- When DMACFG is set to 1, DMA is in circular mode
  - DMA programming is in circular mode or double-buffer mode
  - In this mode, when ADC conversion is started again and the converted data is valid, a DMA request will be generated

24.4.11 Simulating a window watchdog

The function of the simulated window watchdog is enabled by the AWDEN bit of register ADC_CF1. When the analog window watchdog function needs to be used, the values of the high threshold AWDHT[11:0] and low threshold AWDLT[11:0] of the register ADC_AWDT need to be configured, and the fluctuation range of the voltage value sampled by the ADC channel can be set as required.

When single-channel ADC sampling is used, AWDCHEN of register ADC_CFG1 can be set to "1" to enable the analog watchdog function of single channel. In addition, you need to configure the AWDCHSEL bit of the ADC_CFG1 register to select the channel to be sampled, and configure the CHxSEL bit of the ADC_CHSEL register to enable the corresponding channel.

When the configured channel sampling value, that is, the CDATA value of register ADC_DATA is greater than the value of AWDHT[11:0] or less than the value of AWDLT[11:0], the AWDFLG bit of register ADC_STS is set. If the AWDIEN of register ADC_IEN is set, the ADC interrupt is triggered.

If multi-channel sequence sampling is used, the AWDCHEN clear "0" of register ADC_CFG1 is required to enable the analog watchdog function on all channels.

The AWDFLG bit of register ADC_STS is also set when the channel sampling is outside the range of high threshold AWDHT[11:0] and low threshold AWDLT[11:0]. If the AWDIEN of register ADC_IEN is set, ADC interrupt is triggered.

24.4.12 Low-power Characteristics

24.4.12.1 Automatic delay conversion mode

This mode is used to simplify the software and optimize the application program performance during low-speed running, and ADC overrun may occur easily.Set WAITCEN of configuration register ADC_CFG1 to 1, enable the automatic delay conversion mode, and new ADC conversion will start only after the data in ADC data register are read, which is a method of adaptive ADC speed and adaptive system reading ADC data speed.

24.4.12.2 Automatic shutdown mode

This mode can greatly reduce the application power consumption, and is suitable for applications with relatively few conversions or long conversion request time interval. Automatic shutdown mode can be used in combination with automatic delay conversion mode in low-frequency application.

Automatic shutdown mode can be enabled by setting AOEN bit of configuration register ADC_CFG1 to 1. When AOEN bit is set to 1 and there is no ADC conversion, it will be powered off automatically, and when the conversion is started, ADC will be waken up automatically.

24.5 Register Address Mapping

Table 89 ADC Register Address Mapping

Register name	Description	Offset address
ADC_STS	ADC state register	0x00
ADC_IEN	ADC interrupt enable register	0x04
ADC_CTRL	ADC control register	0x08
ADC_CFG1	ADC configuration register 1	0x0C
ADC_CFG2	ADC configuration register 2	0x10
ADC_SMPTIM	ADC sampling time register	0x14
ADC_AWDT	ADC watchdog threshold register	0x20
ADC_CHSEL	ADC channel selection register	0x28
ADC_DATA	ADC data register	0x40
ADC_CCFG	ADC common configuration register	0x308

24.6 Register Functional Description

24.6.1 ADC state register

Offset address: 0x00

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ADCRDYFLG	RC_W1	ADC Ready Flag 0: ADC not ready 1: ADC has been ready to start conversion
1	EOSMPFLG	RC_W1	End of Sampling Flag This bit is set to 1 by hardware and cleared by software 0: Not in the phase of end of sampling 1: Reach the condition for end of sampling phase
2	EOCFLG	RC_W1	End of Conversion Flag This bit is set to 1 by hardware and cleared by software or read the value of ADC_DATA to clear 0 0: Conversion does not end 1: Conversion ends
3	EOSEQFLG	RC_W1	End of Sequence Flag This bit is set to 1 by hardware and cleared by software 0: Sequence conversion not completed 1: Sequence conversion completed
4	OVREFLG	RC_W1	ADC Overrun Event Flag This bit is set to 1 by hardware and cleared by software 0: No overrun event 1: Overrun event occurred
6:5	Reserved		
7	AWDFLG	RC_W1	Analog Watchdog Flag This bit is set to 1 by hardware and cleared by software, indicating whether an analog watchdog event occurs. 0: Not occur 1: Occurred
31:8	Reserved		

24.6.2 ADC interrupt enable register (ADC_IEN)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ADCRDYIEN	R/W	ADC Ready Interrupt Enable 0: Disable 1: Enable
1	EOSMPIEN	R/W	End of Sampling Flag Interrupt Enable 0: Disable 1: Enable
2	EOCIEN	R/W	End of Conversion Interrupt Enable 0: Disable 1: Enable
3	EOSEQIEN	R/W	End of Conversion Sequence Interrupt Enable 0: Disable 1: Enable
4	OVRIEN	R/W	Overrun Interrupt Enable 0: Disable 1: Enable

Field	Name	R/W	Description
6:5	Reserved		
7	AWDIEN	R/W	Analog Watchdog Interrupt Enable 0: Disable 1: Enable
31:8	Reserved		

Note: Changing the value of the ADC_IEN register is allowed only when STARTCEN=0.

24.6.3 ADC control register (ADC_CTRL)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	ADCEN	R/S	ADC Enable This bit is set to 1 by software and cleared by hardware. 0: ADC is disabled 1: ADC is enabled Note: ADCEN bit can be set by software only when all bits of ADC_CTRL register are 0.
1	ADCD	R/S	ADC Disable This bit is set to 1 by software and cleared by hardware. 0: Invalid 1: Disable ADC, and enter power-off mode Note: ADCD bit can be set by software only when ADCEN=1 and STARTCEN=0.
2	STARTCEN	R/S	ADC Start Conversion Enable This bit is set to 1 by software and cleared by hardware. 0: ADC conversion is disabled 1: Start ADC conversion Note: STARTCEN bit can be set by software only when ADCEN=1 and ADCD=0.
3	Reserved		
4	STOPCEN	R/S	ADC Stop Conversion Enable This bit is set to 1 by software and cleared by hardware. 0: Invalid 1: Stop ADC conversion Note: This bit can be set by software only when STARTCEN=1 and ADCD=0.
30:5	Reserved		
31	CAL	R/S	ADC Calibrate This bit is set to 1 by software and cleared by hardware. 0: Calibration is completed 1: Start calibration Note: CAL bit can be set by software only when ADC is disabled.

24.6.4 ADC configuration register 1 (ADC_CFG1)

Offset address: 0x0C

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	DMAEN	R/W	DMA Enable 0: DMA is disabled 1: DMA is enabled Note: The software allows writing this bit only if STARTCEN=0.
1	DMACFG	R/W	DMA Mode Configure This bit is valid only when DMAEN=1. 0: DMA single mode 1: DMA circular mode
2	SCANSEQDIR	R/W	Scan Sequence Direction Configure 0: Scan forward (from CHSEL0 to CHSEL16) 1: Scan backward (from CHSEL16 to CHSEL0)
4:3	DATARESCFG	R/W	Data Resolution Configure 00: 12 bits 01: 10 bits 10: 8 bits 11: 6 bits
5	DALIGCFG	R/W	Data Alignment Configure 0: Right alignment 1: Left alignment
8:6	EXTTRGSEL	R/W	External Trigger Event Select These bits are used to select the external event for triggering ADC conversion. 000: Event 0 001: Event 1 010: Event 2 011: Event 3 100: Event 4 101: Event 5 110: Event 6 111: Event 7
9	Reserved		
11:10	EXTPOLSEL	R/W	External Trigger Enable and Polarity Select 00: Hardware trigger detection is disabled (conversion can be started by software) 01: Hardware trigger detected on rising edge 10: Hardware trigger detected on falling edge 11:: Hardware trigger detected on both rising and falling edges
12	OVRMAG	R/W	Overrun Management Mode 0: When an overrun event is detected, ADC_DATA register saves previous data 1: When an overrun event is detected, ADC_DATA register saves the last converted data
13	CMODESEL	R/W	Select Single/Continuous Conversion Mode 0: Single conversion mode 1: Continuous conversion mode
14	WAITCEN	R/W	Wait Conversion Mode Enable 0: Disable 1: Enable
15	AOEN	R/W	Auto-Off Mode Enable 0: Disable 1: Enable

Field	Name	R/W	Description
16	DISCEN	R/W	Discontinuous Mode Enable 0: Disable 1: Enable
21:17	Reserved		
22	AWDCHEN	R/W	Enable The Watchdog On A Single Channel or on All Channels 0: Enable analog watchdog on all channels 1: Enable analog watchdog on a single channel
23	AWDEN	R/W	Analog Watchdog Enable 0: Disable 1: Enable
25:24	Reserved		
30:26	AWDCHSEL	R/W	Analog Watchdog Channel Select These bits are used to configure the input channel for the analog watchdog to monitor ADC 00000: Channel 0 00001: Channel 1 ..... 10010: Channel 18 Other values: Reserved, not used Note: The channel selected by AWDCHSEL bit must be written in CHSELR register
31	Reserved		

Note: These bits can be rewritten only when STARTCEN=0 (confirming no ongoing conversion).

24.6.5 ADC configuration register 2 (ADC_CFG2)

Offset address: 0x10

Reset value: 0x0000 0000

Field	Name	R/W	Description
29:0	Reserved		
31:30	CLKCFG	R/W	ADC Clock Mode Configure 00: ADCCLK (asynchronous clock mode) 01: PCLK/2 (synchronous clock mode) 10: PCLK/4 (synchronous clock mode) 11: Reserved Note: The software allows writing these bits only when ADC is disabled.

24.6.6 ADC sampling time register (ADC_SMPTIM)

Offset address: 0x14

Reset value: 0x0000 0000

Field	Name	R/W	Description
2:0	SMPCYCSEL	R/W	Sampling Cycles Selecte 000: 1.5ADC clock cycles 001: 7.5ADC clock cycles 010: 13.5ADC clock cycles 011: 28.5ADC clock cycles 100: 41.5ADC clock cycles 101: 55.5ADC clock cycles 110: 71.5ADC clock cycles 111: 239.5ADC clock cycles Note: These bits can be rewritten only when STARTCEN=0.
31:3	Reserved		

24.6.7 ADC watchdog threshold register (ADC_AWDT)

Offset address: 0x20

Reset value: 0x0FFF 0000

Field	Name	R/W	Description
11:0	AWDLT[11:0]	R/W	Analog Watchdog Low Threshold
15:12	Reserved		
27:16	AWDHT[11:0]	R/W	Analog Watchdog High Threshold
31:28	Reserved		

Note: These bits can be rewritten only when STARTCEN=0.

24.6.8 ADC channel selection register (ADC_CHSEL)

Offset address: 0x28

Reset value: 0x0000 0000

Field	Name	R/W	Description
17:0	CHxSEL	R/W	Channel-x Select 0: Input channel x is not selected as conversion channel 1: Input channel x is selected as conversion channel
31:18	Reserved		

Note: These bits can be rewritten only when STARTCEN=0.

24.6.9 ADC data register (ADC_DATA)

Offset address: 0x40

Reset value: 0x0000 0000

Field	Name	R/W	Description
15:0	CDATA	R	Converted Data These bits are read-only. Include the conversion result values of last conversion channel. CDATA[6:0] value is calibration factor only when calibration is completed.
31:16	Reserved		

24.6.10 ADC common configuration register (ADC_CCFG)

Offset address: 0x308

Reset value: 0x0000 0000

Field	Name	R/W	Description
21:0	Reserved		
22	VREFEN	R/W	V_{REFINT} Enable 0: Disable 1: Enable
23	TSEN	R/W	Temperature Sensor Enable 0: Disable 1: Enable
31:24	Reserved		

Note: This bit can be rewritten only when STARTCEN=0

25 Cyclic Redundancy Check Computing Unit (CRC)

25.1 Introduction

The cyclic redundancy check (CRC) computing unit can get 8/16/32-bit CRC computing result by calculating the input data through a fixed generator polynomial, which is mainly used to detect or verify the correctness and integrity of the data after transmission or saving.

25.2 Functional Description

25.2.1 Calculation Method

Use CRC-32 (Ethernet) polynomial: 0x4C11DB7

$(X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1)$

25.2.2 Calculation Time

The calculation time is four AHB clock cycles.

25.2.3 Functional Characteristics

- Handle 8-bit, 16-bit and 32-bit data
- Programmable CRC initial value
- Independent 32-bit input and output register
- Reversible option of I/O data
- The data width can be dynamically adjusted to reduce the number of times of calculating and writing
- The high and low levels of input data can be reversed in order to adapt to different little-endian and big-endian systems
- Word or byte calculation can be performed, depending on the different data formats written.
- Have data buffer to reduce wait cycles

Every time a new data is written, the result will be a combination of the last calculation result and the new calculation result. (Execute operation for the whole word). Write operation of CPU will be suspended during calculation, so that "Back-to-back" write or continuous "read" -"write" operation can be performed for the register CRC_DATA.

25.3 Register Address Mapping

Table 90 CRC Computing Unit Register Address Mapping

Register name	Description	Offset address
CRC_DATA	Data register	0x00
CRC_INDATA	Independent data register	0x04
CRC_CTRL	Control register	0x08

Register name	Description	Offset address
CRC_INITVAL	CRC initial value register	0x10

25.4 Register Functional Description

25.4.1 Data register (CRC_DATA)

Offset address: 0x00

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
31:0	DATA	R/W	32bit Data When the write operation is performed, it is used as a new data input port for CRC calculation. When the read operation is performed, the result of the CRC calculation is returned.

25.4.2 Independent data register (CRC_INDATA)

Offset address: 0x04

Reset value: 0x0000 0000

Field	Name	R/W	Description
7:0	INDATA	R/W	Independent 8bit Data Can be used for temporary storage of 1-byte data. CRC rest generated by RST bit of the register CRC_CTRL has no effect on this register.
31:8	Reserved.		

Note: This register does not take part in calculation and can store any data.

25.4.3 Control register (CRC_CTRL)

Offset address: 0x08

Reset value: 0x0000 0000

Field	Name	R/W	Description
0	RST	R/S	Reset CRC Calculation Unit Set the data register to 0xFFFF FFFF. It can only set this bit, which shall be automatically cleared by hardware. 0: Invalid operation 1: Reset register CRC_DATA
4:1	Reserved		
6:5	REVI	R/W	Input Data Reverse Reverse the input data in different units. 00: Not reversed 01: In byte 10: In half word 11: In word
7	REVO	R/W	Output Data Reverse 0: Not reversed 1: Reversed

Field	Name	R/W	Description
31:8	Reserved		

25.4.4 Initial value register (CRC_INITVAL)

Offset address: 0x10

Reset value: 0xFFFF FFFF

Field	Name	R/W	Description
31:0	VALUE	R/W	Initial CRC Value The CRC initial value is programmable, and this bit is used to set the CRC initial value.

26 Chip Electronic Signature

The chip electronic signature includes flash capacity information of main memory and 96-bit unique chip ID, which have been written into the system memory area of the chip before leaving the factory, and are read-only and cannot be modified by users.

26.1 Functional Description

Main use of 96-bit chip ID:

- Used as serial number
- As the password, when writing the flash memory, the code and password can be combined by algorithm to improve the security of the code in Flash
- Used for startup configuration
- The reference number provided by the identity is unique to any MCU series. Users cannot change the unique ID under no circumstances. According to different usage, users can choose to read the identity in byte, half-word, or word.

26.2 Register Functional Description

26.2.1 96-bit Unique Chip ID

Base address: 0x1FFF F7AC

Offset address: 0x00

Field	Name	R/W	Description
31:0	U_ID[31:0]	R	Unique identity 31:0 bit

Offset address: 0x04

Read-only, the value has been prepared before leaving the factory

Field	Name	R/W	Description
31:0	U_ID[63:32]	R	Unique identity 63:32 bits

Offset address: 0x08

Read-only, the value has been prepared before leaving the factory

Field	Name	R/W	Description
31:0	U_ID[95:64]	R	Unique identity 95:64 bits

26.2.2 Flash Memory Capacity Register

Base address: 0x1FFF F7CC

Offset address: 0x00

Field	Name	R/W	Description
15:0	F_SIZE	R	Flash memory capacity Indicate the capacity of main memory area of the product (KB). For example: 0x040=64 KB

Field	Name	R/W	Description
23:16	P_Version	R	Product version 0xA1:A1 0xA2:A2 0xB1:B1 … And so on.
27:24	P_Series	R	Product series 0000 : E030 0001 : F030 Other values: reserved
31:28	Reserved		

Note:

（1）P_Version indicates the wafer version -A1/A2/B1. Set this parameter based on the actual situation.

（2）P_Series indicates the product series -E030/F030, there are no other series at present.

27 Version History

Table 91 Document Version History

Date	Version	Change History
November, 2023	1.0	New

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8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.